On-Chip Inductance Cons and Pros

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***Abstract*—This paper provides a high level survey of the increasing effects of on-chip inductance. These effects are classified into desirable and nondesirable effects. Among the undesirable effects of on-chip inductance are higher interconnect coupling noise and substrate coupling, challenges for accurate extraction, the required modifications of the infrastructure of CAD tools, and the inevitably slower CAD tools as compared to *RC*-based tools. Among the desirable effects is lower power consumption, less need for repeaters, faster signal rise time, and less delay uncertainty. The viability of design methodologies considering on-chip inductance is briefly discussed.**

I. Historical Perspective

HISTORICALLY, the gate parasitic impedances have been much larger than the interconnect parasitic impedances since the gate geometries (the width and length) were quite large (about 5 μm was a typical minimum feature size in 1980). Thus, interconnect parasitic impedances have historically been neglected and the interconnect was modeled as a short circuit. With the scaling of the minimum gate feature size, interconnect capacitances have become comparable to the gate capacitance, requiring the interconnect to be modeled as a single lumped capacitance that is added to the gate capacitance. With this interconnect model, new design techniques emerged to drive large capacitive loads associated with long global interconnects and large interconnect trees with high fanout. Cascaded tapered buffers are used to minimize the propagation delay of CMOS gates driving these large capacitive loads e.g., [1] and [2].

With increasing device densities per unit area, the cross-sectional area of interconnects has been reduced to provide more interconnect per unit area. Also, the improved yield of CMOS fabrication processes permits manufacturing larger chips with higher reliability. Thus, the global wires connecting modules across an IC have increased in length. Both the decreased cross-sectional area and the increased wire length have caused the global wire resistances to dramatically increase. The interconnect model now includes the resistance of the interconnect. Including resistance in the interconnect model dramatically changed the design and analysis of integrated circuits, e.g., [3]–[5]. With a short circuit or a capacitive interconnect model, the interconnect could be treated as a single node. However, by including the series resistance, the interconnect is composed of multiple nodes, each node having a different voltage waveform. This characteristic has greatly complicated the analysis of circuits with resistive interconnect. Completely new problems and design techniques have emerged due to the transition from a capacitive to an *RC* model such as *RC* tree analysis techniques, clock skew problems, repeater insertion techniques, power consumption estimation, model order reduction techniques, and IR drops in the power supply, to name a few. Almost every aspect of the design and analysis of integrated circuits was affected by the new interconnect model.

This paper briefly discusses the importance, effects, and issues involved in a transition from an *RC* interconnect model to an *RLC* model which includes the inductance of the interconnect. This transition has the potential to change all aspects of the design and analysis of integrated circuits in analogy to the transition from a capacitive to an *RC* interconnect model. However, unlike the transition from a capacitive to an *RC* model which only resulted into undesirable effects, the increasing inductance effects can have several desirable consequences which are pointed out in the paper.

The rest of the paper is organized as follows. The increasing importance of including inductance in current and future technologies is discussed in Section II. The pros of on-chip inductance are discussed in Section III. The cons of on-chip inductance are discussed in Section IV. Finally, conclusions on the viability of design methodologies including on-chip inductance is discussed in Section V.

II. Importance of Inductance in Current and Future Technologies

On-chip inductance has currently become more important with faster on-chip rise times and wider wires. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistance lines that can exhibit significant inductive effects. Furthermore, performance requirements are pushing the introduction of new materials such as copper interconnect for low resistance interconnect and new dielectrics to reduce the interconnect capacitance. These technological advances increase the importance of inductance. In the limiting case, the advent of high critical-temperature superconductors has created the possibility of realizing high density, extremely high-speed interconnects for integrated circuits. These superconductive interconnects have zero dc resistance and are highly sensitive to inductance. These interconnects are best modeled as lossless transmission lines.

On-chip inductance can cause significant errors in current deep submicron technologies. For example, three sets of AS/X [6] simulation results are presented based on IBM's most recent technology to illustrate the importance of on-chip self and mutual inductances. The first example is a 4-bit coupled bus (see Table I). The second example is a tree coupled with two lines (see Table II). And the third example is a pair of lines coupled with each other (see Table III). In all three examples simulations are done for three cases. In case I, self and mutual inductances are not included. That is, signal lines are considered as standard

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TABLE I
AS/X SIMULATION OF A 4-BIT BUS

BUS	All lines are switching in the same direction.				
	Case			% Deviation	
	I	II	III	I- III	II-III
Delay (ps)	29.32	44.2	58.67	100	33
Rise Time (ps)	84.59	25.5	26.81	68.3	5.14
% Overshoot	0	10.3	23.79	-	126
Time of overshoot	-	115	155.2	-	35.3

TABLE II
AS/X SIMULATION OF A COUPLED TREE NETWORK

TREE	All lines are switching in the same direction.				
	Case			% Deviation	
	I	II	III	I- III	II-III
Delay (ps)	30.46	43.59	51.98	71.5	18.5
Rise Time (ps)	87.1	43.36	37.29	58.6	13.4
% Overshoot	0	7.2	15	-	108
Time of overshoot	-	113.4	134	-	18.2

TABLE III
AS/X SIMULATION OF A PAIR OF COUPLED LINES

LINE	All lines are switching in the same direction.				
	Case			% Deviation	
	I	II	III	I- III	II-III
Delay (ps)	63.12	74.13	83.64	32.53	12.83
Rise Time (ps)	147.8	85.36	49	67	43
% Overshoot	0	0.74	6.2	-	737
Time of overshoot	-	269	221.5	-	17.69

RC lines with coupling capacitances only. In case II, self-inductance is included, and lines are considered as *RLC* lines with coupling capacitance, but no coupling inductance. In case III, both self and mutual inductances are included and lines are considered as *RLC* lines with coupling capacitance and mutual inductance. Results show that the error due to neglecting inductance can be more than 100% for the delay calculation and 70% in the rise time. What makes these errors even more serious is that neglecting inductance and using an *RC* model always results in underestimating the propagation delay (e.g., see Fig. 1). Thus, VLSI circuits designed using an *RC* interconnect model may not satisfy the assigned performance targets despite a worst case analysis being applied in the circuit design process.

In general, there are two factors controlling the error between an *RC* and an *RLC* model. These two factors are the damping factor of an *RLC* line and the ratio between the input signal rise time to the time of flight of signals across the line [8]. The damping factor of an *RLC* line is given by

$$\xi = \frac{Rl}{2}\sqrt{\frac{C}{L}} \tag{1}$$

where R, L, and C are the resistance, inductance, and capacitance per unit length of the line, respectively, and l is the length

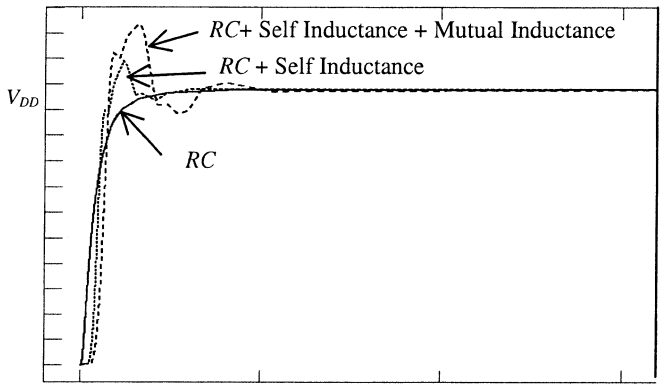

Fig. 1. Signal behavior on one net of a 4-bit BUS.

of the line. The damping factor of the line represents the degree of attenuation the wave suffers as it propagates a distance equal to the length of the line. As this attenuation increases, the effects of the reflections decrease and the *RC* model becomes more accurate. Note that the damping factor is proportional to the length of the line and thus very long lines will exhibit less inductance effects. Alternatively, the damping factor can be expressed as

$$\xi = \frac{R_t C_t}{2\sqrt{L_t C_t}} = \frac{\tau_{RC}}{2\tau_{LC}} \tag{2}$$

where R_t, L_t, and C_t are the total resistance, inductance, and capacitance of the line, respectively, and τ_{RC} and τ_{LC} are the *RC* and *LC* time constants of the line. This relation illustrates the "fight" between the *RC* and *LC* time constants of the line. A reduction in the *RC* time constant results in a direct increase in the inductance effects exhibited by the line. Note that many of the technological advancements that have been achieved or are still in development target reducing the *RC* time constant. Examples are copper interconnect, dielectrics with lower ε_r, and superconductive interconnects. Also, many of the design methodologies used to reduce the delay of critical lines concentrates mainly on reducing the *RC* time constant of the line, such as using wider wires, wider drivers, and repeater insertion. In the limit, if the *RC* time constant of a line is sufficiently reduced, the line will behave as a lossless transmission line and signals can be transmitted across the line with the speed of light.

The other factor determining inductance effects is the ratio between the input signal rise time to the time of flight of signals across the line and is given by

$$\frac{t_r}{2l\sqrt{LC}} \tag{3}$$

where t_r is the rise time of the input signal. As this ratio increases, the line can be more accurately modeled as an *RC* line. Note that in this case the relation implies that shorter lines will suffer less inductance effects mainly because the rise time of the input signal will override the *LC* time constant. Hence, there is a range of the length of the interconnect for which inductance effects are significant with very short and very long lines suffering no inductance effects [8]. Note that the rise times of input signals to the interconnect are becoming faster all the time with technology scaling, increasing inductance effects in future technologies. Even if some techniques can be applied today to

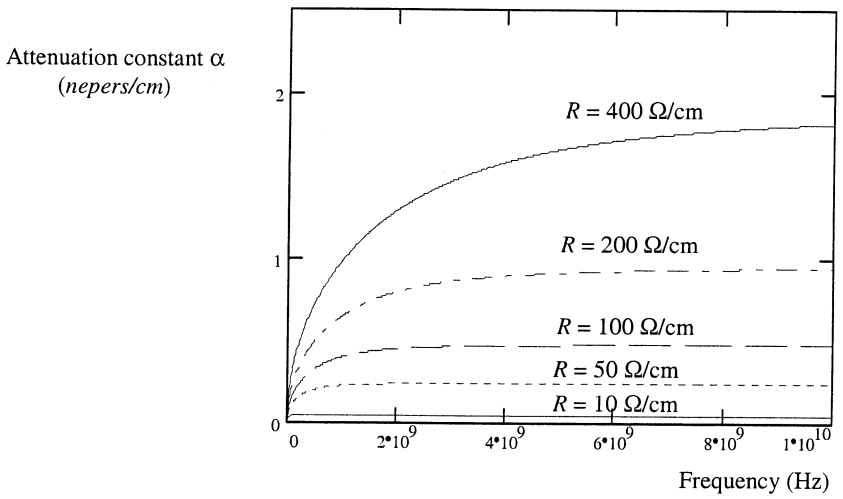

Fig. 2. The attenuation constant versus frequency: $L = 10$ nH/cm, $C = 1$ pF/cm, and R is 10, 50, 100, 200, and 400 Ω/cm, respectively.

reduce the effect of inductance allowing the use of the well-developed *RC*-based CAD tools, inductance effects will be very hard to suppress or ignore in future technologies and CAD tools have to be modified to include the effect of inductance.

Equivalent figures of merit for trees were developed in [9] to characterize the importance of on-chip inductance. These expressions at node i of a tree are given by

$$\zeta_i = \frac{1}{2}\frac{\sum_k C_k R_{ik}}{\sqrt{\sum_k C_k L_{ik}}} \tag{4}$$

and

$$\frac{t_r}{2\sqrt{\sum_k C_k L_{ik}}} \tag{5}$$

respectively, where R_{ik} (L_{ik}) is the common resistance (inductance) from the input of the tree to nodes i and k and k runs over all the capacitances in the tree.

III. Pros of On-Chip Inductance

This section briefly discusses the desirable effects of inductance on the performance of integrated circuits. The effects of inductance on signal rise time, repeater insertion process, power consumption, and delay uncertainty are discussed.

A. Effects of Inductance on the Signal Rise Time

The rise time of signals propagating across *RLC* lines improves as the inductance effects of the line increase. This behavior can be explained by referring Fig. 2 which depicts the attenuation of signals as they travel across an *RLC* line as a function of frequency. Higher frequency components at the edges of a pulse suffer greater attenuation as compared to low frequency components. The shape of a signal degrades as the signal travels across a lossy transmission line due to the loss of these high frequency components. The attenuation constant becomes less frequency dependent as inductance effects increase or as $R/\omega L$ decreases as shown in Fig. 2. In the limiting case of a lossless line representing maximum inductance effects, the attenuation constant α is zero. Thus, as inductance effects increase, a pulse propagating across an *RLC* line maintains the high frequency components in the edges, improving the signal rise and fall times.

B. Effects of Inductance on the Repeater Insertion Process

Repeater insertion has become a common design methodology for driving long resistive interconnect, e.g., [3]–[5]. Since the *RC* time constant of a line is given by $R_t C_t = RCl^2$ and has a square dependence on the length of the line, subdividing the line into shorter sections by inserting repeaters is an effective strategy for reducing the total propagation delay. Currently, typical high performance circuits have a significant number of repeaters inserted along global interconnect lines. These repeaters are large gates and consume a significant portion of the total circuit power.

A general expression for the propagation delay from the input to the output of an *RLC* line of length l with an ideal power supply and an open circuit load is given by [7]

$$t_{pd} = \sqrt{LC}(e^{-2.9(\alpha_{asym} l)^{1.35}} l + 0.74\alpha_{asym} l^2) \tag{6}$$

where

$$\alpha_{asym} = \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{7}$$

α_{asym} is the asymptotic value at high frequencies of the attenuation per unit length of the signals as the signals propagate across a lossy transmission line as shown in Fig. 2.

For the limiting case where $L \to 0$, (6) reduces to $0.37RCl^2$, illustrating the square dependence on the length of an *RC* wire as aforementioned. For the other limiting case where $R \to 0$, the propagation delay is given by $\sqrt{L_t C_t} = l\sqrt{LC}$. Note the linear dependence on the length of the line.

As discussed in Section I, the amount of inductance effects present in an *RLC* line depends on the ratio between the *RC* and the *LC* time constants of the line. Hence, as inductance effects increases, the *LC* time constant dominates the *RC* time constant

TABLE IV
THE TOTAL REPEATER AREA, TOTAL POWER, AND TOTAL MAXIMUM PATH DELAY OF ALL OF THE TREES. THE PERCENT SAVINGS SHOWN HERE REPRESENT THE AVERAGE SAVINGS IN AREA, POWER, AND MAXIMUM PATH DELAY WHEN USING AN *RLC* MODEL FOR REPEATER INSERTION

	Totals				
	Un-Buffered	Savings in delay	Buffered *RLC* Model	Savings compared to *RC*	Buffered *RC* Model
Area (min inverters)	0	-	14116	40.8%	23854
Max delay (ps)	6554	42.2%	3787	6.7%	4061
Power (PJ/Cycle)	-	-	1379	15.6%	1632

and the delay of the line changes from a quadratic to a linear dependence on the line length [7]. As a consequence, the optimum number of repeaters for minimum propagation delay decreases as inductance effects increase. In the limit, an *LC* line requires *zero* repeater area to minimize the overall propagation delay.

Inserting repeaters based on an *RC* model and neglecting inductance results in a larger repeater area than necessary to achieve a minimum delay. The magnitude of the excess repeater area when using an *RC* model depends upon the relative magnitude of the inductance within the *RLC* tree. The reduced number of inserted repeaters also simplifies the layout and routing constraints. Also, the reduced repeater area greatly reduces the power consumed by the repeaters in an integrated circuit. A more thorough analytical analysis of the effect of inductance on the repeater insertion process can be found in [7]. Practical data are listed in Table IV for repeaters inserted in a large number of typical copper interconnects from a 0.25 μm CMOS technology [10]. Note that by using an *RLC* model rather than an *RC* model, a better delay can be achieved with significantly less repeater area and power consumption by the repeaters.

C. Effects of Inductance on Power Dissipation

Power consumption is an increasingly important design parameter with mobile systems and high performance, high complexity circuits such as leading edge microprocessors. If the frequency of switching is f cycles per second, then the dynamic power consumption is described by the well-known formula,

$$P_{dyn} = C_t V_{DD}^2 f. \tag{8}$$

The dynamic power depends only on the total load capacitance, the supply voltage, and the operating frequency. As discussed in Section III-B, increasing inductance effects result in fewer number of repeaters as well as smaller repeater size. The smaller size and number of repeaters, therefore, significantly reduces the total capacitance of the repeaters and, consequently, reduces the total dynamic power consumption.

The short-circuit power results from the NMOS and PMOS blocks of a CMOS gate being on simultaneously during the rise and fall times of the input signal, creating a current path between the power supply and ground. As discussed in Section III-A, the inductance reduces the rise time of the signals in an integrated circuit, reducing the short-circuit power. The short circuit power consumption of a gate driven by an *RLC* line versus the line inductance is plotted in Fig. 3. Note that as inductance effects increase, the short-circuit power consumption significantly decreases due to the faster input rise time. Also, the smaller repeater sizes dramatically reduces the short-circuit power consumption since the short circuit power of a CMOS gate is super linearly dependent on the transistor widths. Finally, it has been shown in [11] that the short-circuit power consumption of a CMOS gate decreases as the inductance of the driven net becomes more significant. Intuitively, inductance is an element which does not consume any power while resistance consumes power. Hence, as the interconnect behavior becomes dominated by inductance rather than resistance, the power consumption of integrated circuits will be reduced.

D. Effects of Inductive Coupling on Delay Uncertainty

In a set of inductively and capacitively coupled lines, the signal propagation delay on a particular line is minimum when neighbor lines are switching in the same direction. The delay on that line is maximum when that particular line is switching in opposite direction to neighbor lines due to the increased effective capacitance that has to be charged or discharged. The ratio of the maximum and minimum signal delay on a certain signal line can be defined as *delay uncertainty* D_U for that line as given by

$$D_U = \frac{t_{d_{\max}}}{t_{d_{\min}}}. \tag{9}$$

For *RLC* lines, the delay is given by [12]

$$t_d = 1.047 \cdot E \cdot \tau_{LC} + 1 \cdot 4 \cdot \tau_{RC} \tag{10}$$

where E is a term that depends on the damping factor of this line as described in [12] and

$$\tau_{RC} = \sum_k \left[R_k \cdot \sum_{r,j} C_{rj} \cdot (\alpha_r - \alpha_j) \right] \tag{11}$$

$$\tau_{LC} = \sqrt{\sum_k \left[L_k \sum_{r,j} C_{rj} (\alpha_r - \alpha_j) + M_k \sum_{l,m} C_{lm} (\alpha_l - \alpha_m) \right]}. \tag{12}$$

Each line has a switching factor associated with it and is denoted α_i for interconnect i. The switching factor takes the values 1, 0, and -1 for lines switching from low-to-high, nonswitching lines, and lines switching from high-to-low, respectively. k runs over all the branches on the path from the primary input to node

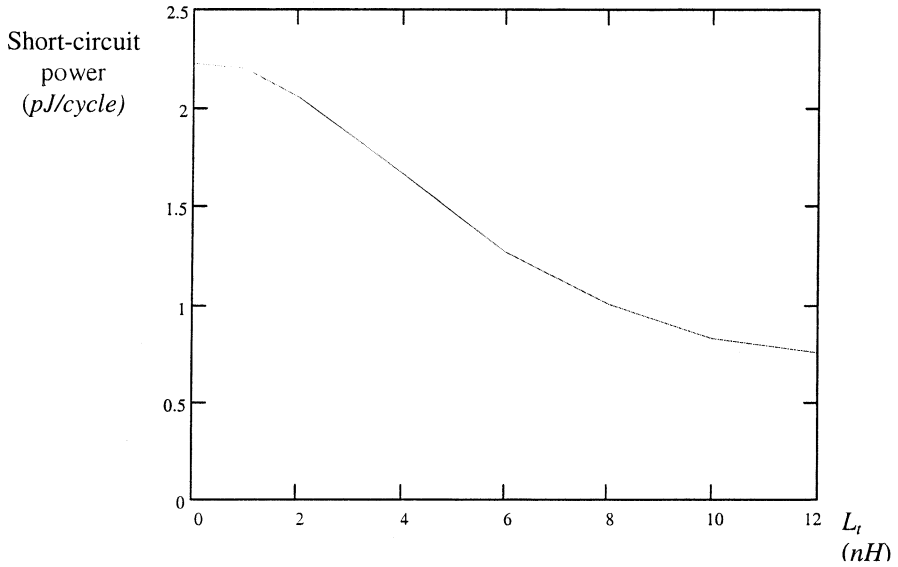

Fig. 3. The short-circuit energy consumed per cycle by CMOS gate driven by an *RLC* line versus the inductance of the line. The total resistance and capacitance of the line are maintained constant at 100 Ω and 1 pF, respectively.

i on the tree which i belongs to; r runs over all the nodes downstream of k on that tree, and j runs over all the nodes to which r has a capacitance connected to. In the case of capacitances to ground, $j = 0$. The index l runs over all the nodes downstream of M_k **on the coupled tree** (which i does not belong to). The index m runs over all the nodes which l has a capacitance connected to.

The time constants τ_{RC} and τ_{LC} depend on the switching directions of neighbor lines. As neighbor lines switch in opposite directions to the line in consideration, τ_{RC} is maximum. When neighbor lines switch in the same direction, τ_{RC} is minimum as given by (11). On the other hand, τ_{LC} decreases when neighbor lines switch in opposite directions due to the opposite currents in neighbor lines, which causes negative mutual inductance terms to appear in (12). When neighbor lines switch in the same direction, τ_{LC} increases since the mutual inductances add to the self inductance as in (12). This opposite behavior of τ_{RC} and τ_{LC} results in reducing the discrepancy between the maximum and minimum delays of a line due to coupling with other lines.

AS/X simulation (Fig. 4.) for the signal on the middle line of three coupled lines shows that as inductance effects increase the ratio between the maximum and minimum delays decreases. That is, higher inductive effects lead to lower delay uncertainty and narrower switching windows. Lowering delay uncertainty is a positive effect of inductance since narrower switching windows gives significant degrees of freedom in physical design to limit noise and control glitches among many other benefits.

IV. Cons of On-Chip Inductance

This section briefly discusses the undesirable effects of inductance on the performance of integrated circuits and on CAD tools performance. The problems of inductance extraction, inductance effects on noise and substrate coupling, and requirements on CAD tools and their performance are discussed.

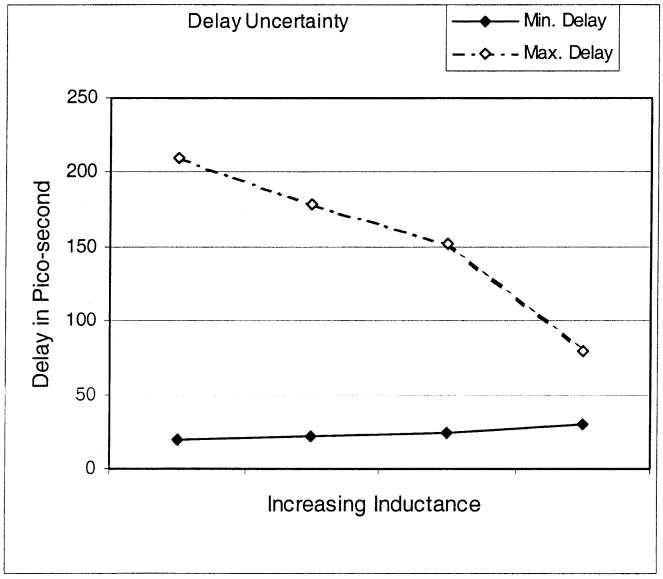

Fig. 4. Delay uncertainty dependence on inductance effects. The data shown is for the delay of the middle line of three coupled parallel lines.

A. Inductance Extraction Challenges

Each interconnect line has an associated self-inductance and an associated mutual inductance to other lines in the circuit. Unlike the resistance and capacitance of interconnect lines, both self and mutual inductances are loop quantities, and they can be determined only if the whole current loop is known; i.e., the exact path in which the current returns to the source is known. The self-inductance of a loop is defined as the flux linked through the loop due to the variation in the current flowing in the loop divided by the value of the current. The current loop also has corresponding coupling inductances that couple the current loop to surrounding current loops. The coupling inductance is the flux caused by an aggressor loop

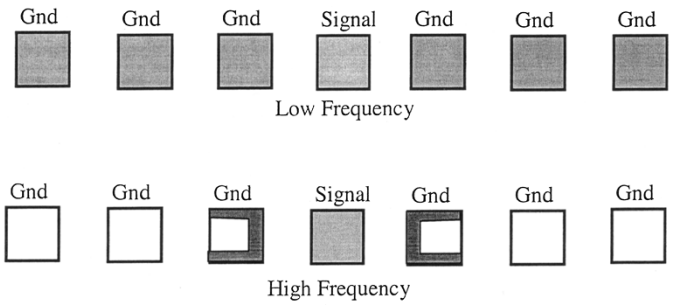

Fig. 5. Frequency dependence of current distribution across signal and ground lines.

linked to a given loop divided by the value of the aggressor current [14].

The current return path is frequency dependent. At low frequency, the inductive impedance (ωL) is less than the resistive impedance (R). Hence, the current tries to minimize the interconnect impedance and thus tries to minimize the interconnect resistance. This causes the current to use as many returns as possible to have parallel resistances, as shown in Fig. 5 [14]. However, at high frequency $\omega L > R$ and the current tries to minimize interconnect impedance by minimizing the loop inductance. This causes the current to use the closest possible return path to form the smallest possible loop inductance, as shown in Fig. 5 [14]. The current would be confined to the nearest possible return only at ultra-high frequencies (higher than 20 GHz) [15]. Therefore, at current clock frequencies, current can spread into a number of the possible current return paths. This behavior makes the extraction of inductance a nontrivial task as it tremendously increases the number of surrounding interconnects that have to be considered.

In order to limit the complexity of the problem, the inductance can be approximated [16] by assuming that the current return path is limited to the nearest power or ground line. Other approaches such as in [17] incrementally improves the accuracy by adding more ground lines to the return path until the extracted inductance is accurate enough. One way to go around the prerequisite of knowing the actual current return paths beforehand is by using the three-dimensional (3-D) field solver. A common approach that is used by 3-D solvers is to extract inductance by applying a finite difference or finite element method to the governing Maxwell equations in differential form. Such an approach generates a global 3-D mesh for all parts of analyzed structure and for surrounding external space. This causes the number of unknowns to increase significantly, and thus a very large linear system can be generated. Solving this large linear system requires excessive memory and consumes long CPU time, which makes inductance extraction of complex 3-D structures using finite element or finite difference methods impractical.

The other approach used in inductance extraction employs the Partial Element Equivalent Circuit method (PEEC) [21], [22]. Using PEEC, only the volume of the conductors needs to be discretized. Thus, using the PEEC method produces a fewer number of unknowns than finite elements and differences. The integral formulation of the PEEC method is used in the widely known MIT inductance extraction program, FastHenry [20].

Hence, inductance extraction is a nontrivial process. However, there are two characteristics of on-chip inductance that can be exploited to simplify the extraction process of on-chip inductance. First, the sensitivity of a signal waveform to errors in the inductance values is low compared to sensitivity to errors in resistance and capacitance values, particularly the propagation delay and rise time. Second, the value of the on-chip inductance is a slow varying function of the width of the wire and the geometry of the surrounding wires [23].

The first characteristic can be explained by the fact that inductance only appears under a square root function in a waveform or timing expression characterizing a signal. The reason for this square root dependence is physical since an *LC* constant has the dimensions of time squared, where L and C are any inductance and capacitance values in the circuit, respectively. The square root dependence can be compared to the linear dependence of the delay expressions on the resistance since any *RC* constant has the dimensions of time, where R is any resistance of the circuit. For example, according to the equivalent Elmore delay for *RLC* trees that was introduced in [13], the 50% delay of the signal at node i of an *RLC* tree is

$$t_{pdi} = 1.047 \cdot \sqrt{\sum_k C_k L_{ik}} \cdot e^{-\zeta_i/0.85} + 0.695 \cdot \sum_k C_k R_{ik} \quad (13)$$

where ζ_i is the damping factor at node i and is

$$\zeta_i = \frac{1}{2} \frac{\sum_k C_k R_{ik}}{\sqrt{\sum_k C_k L_{ik}}}. \quad (14)$$

Note that inductance only appears under a square root. This fact is also evident in (6) and (12).

As an example, AS/X [6] simulations are performed for an *RLC* tree with no inductance (an *RC* model), and with all of the inductance values increased by 10%, 20%, and 30%. These simulations are depicted in Fig. 6. Note in the simulations that using an approximate inductance estimation greatly improves the accuracy of the waveform as compared to using an *RC* model. Even with a 30% error in the inductance values, the propagation delay differs by 9.4% from the actual value as compared to 51% if an *RC* model is used. The improvement in the rise time is even greater. The rise time differs from the actual value by 5.9% with a 30% error in the inductance values as compared to a 71% error when an *RC* model is used. The maximum error in the waveform shape occurs around the overshoots (see Fig. 6). However, estimating the overshoot requires less accuracy since the overshoot is usually evaluated to decide if the overshoot is within an acceptable limit. This high tolerance of the delay expressions to errors in the extracted inductance combined with the slow variation of extracted inductance values with changes in geometry encourage the use of simplified techniques with higher computational efficiency to extract the on-chip inductance.

B. Interconnect and Substrate Coupling Noise

As discussed in Section IV-A, a line can inductively couple to lines that are far away unlike capacitive coupling which only occurs between adjacent lines. The problem of inductive coupling

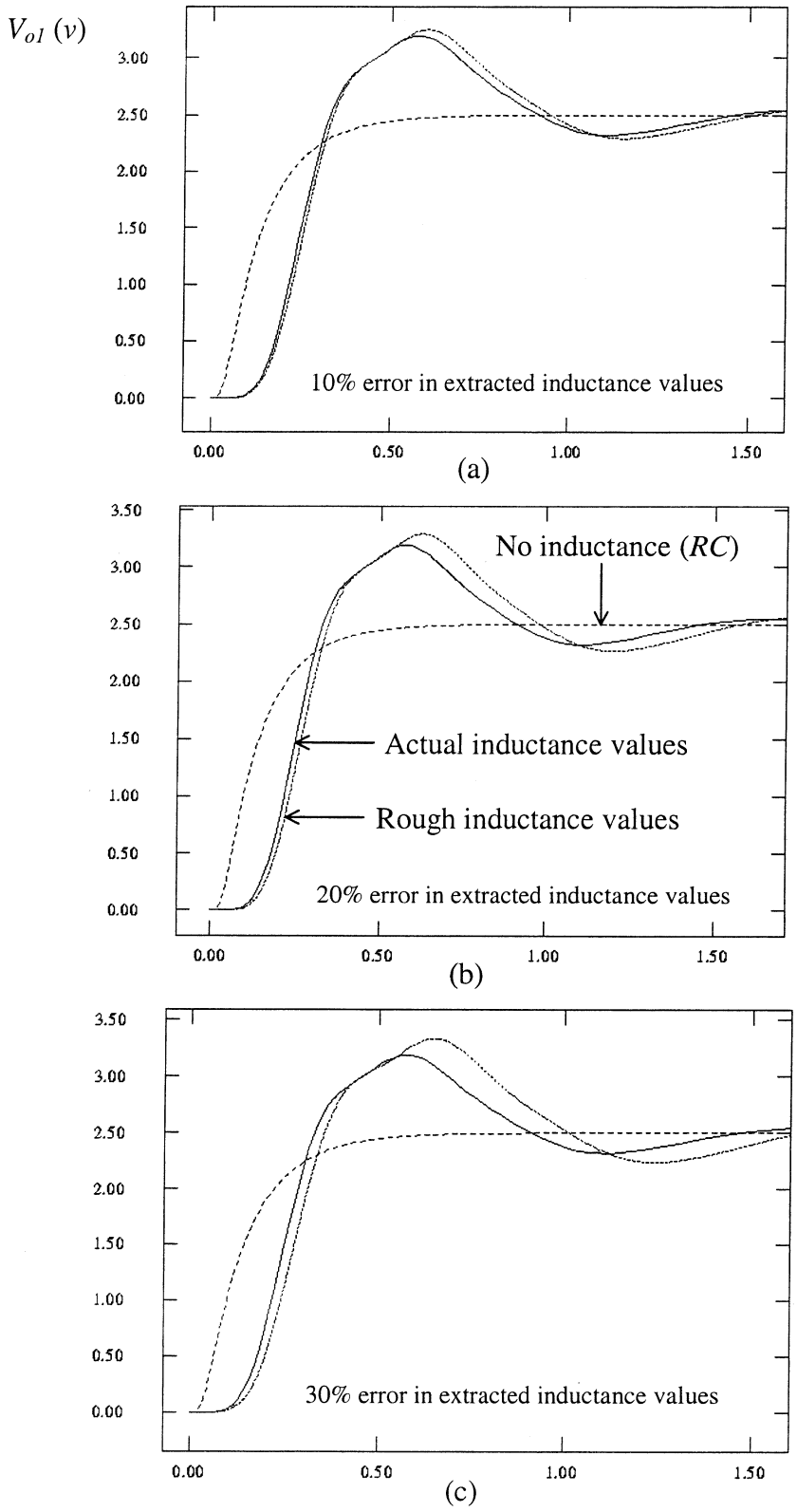

Fig. 6. AS/X simulations of an *RLC* tree with the actual inductance values, with no inductance (an *RC* model), and with all of the inductance values increased by (a) 10%, (b) 20%, and (c) 30%.

is particularly severe in wide busses, which are commonplace in most digital integrated circuits such as DSP and microprocessor circuits. The width of busses in digital circuits is continuously increasing with technology scaling. Hence, the problem of inductive coupling in busses will have even more significance in future technologies.

Physically, a wide bus with all the lines switching in the same direction behaves as one wide line. Such a wide line has much

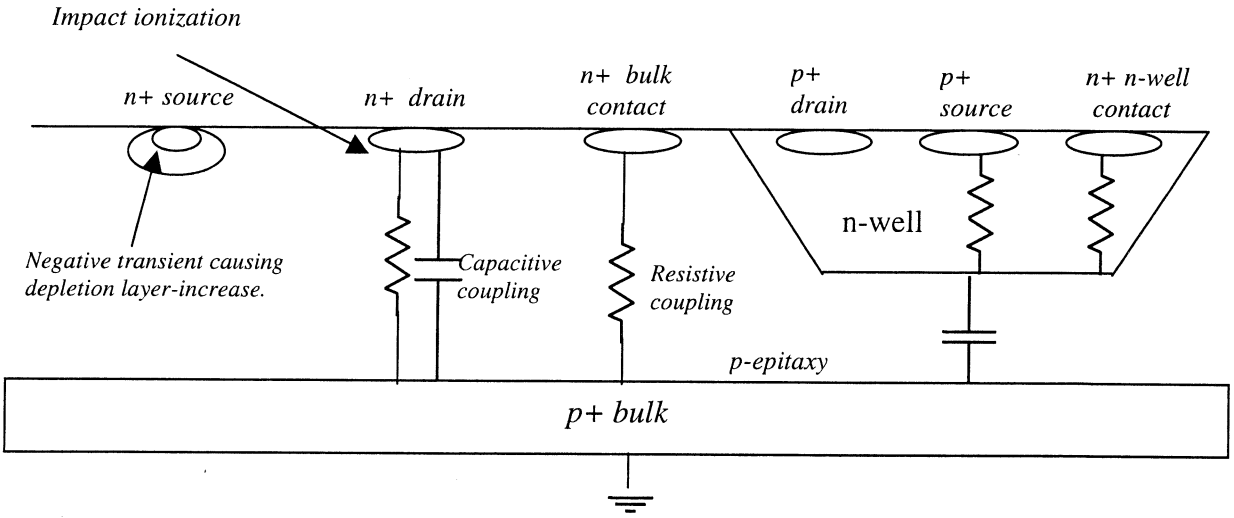

Fig. 7. Mechanisms of substrate noise propagation in an integrated circuit.

higher inductance effects as compared to any of the individual lines in the bus. Hence, the effective inductance of a line that is part of a bus is far larger than the self-inductance of that line. This fact can also be quantitatively understood by referring to (12), which shows that if all the lines are switching in the same direction, the *LC* time constant of the line becomes much larger than the case of an individual line because of all the mutual terms adding to the self inductance term. This increase in the *LC* time constant means much higher overshoots and inductive noise on any line in the bus.

In order to examine the impact of inductance on circuit cross talk in a high-performance 0.18 μm process, the worst case noise generated on an 8-bit, 3000-μm long, standard data bus was simulated in [14], [18]. The bus was implemented in metal 6 with all lines having a metal width of 3 μm and a metal-to-metal spacing of 1.5 μm consistent with typical high-level metal implementations of high-performance global busses. The data bus was also sandwiched between a V_{dd} line and a *GND* line each 15 μm wide to provide a return path for the current flowing in the buses. The drivers and receivers were implemented using simple buffers. A distributed *RLC* model for the interconnect was produced where FastCap [19] was used to model the inter connect capacitance, and FastHenry [20] was used to model both the resistance and the inductance of the interconnects. By applying a 5 ps rise time step signal to all the inputs except the one in the middle, SPICE simulations show a totally unacceptable voltage glitch of 1.17 V. Such a glitch could cause erroneous switching and logic failures. Note that if the inductance is neglected and not modeled, the crosstalk noise becomes only 0.59 V, which is almost *half* the value of the actual glitch. This shows the importance of modeling on-chip inductance for accurate detection of crosstalk voltage glitches.

In terms of substrate coupling, inductance effects increase this type of noise significantly. Overshoots and undershoots due to inductance cause noise coupling through the common substrate, which is both difficult to measure and difficult to control. Substrate noise-conduction modes can be classified into (a) resistive coupling, (b) capacitive coupling, (c) impact ionization, and (d) body effect (see Fig. 7). All these modes involve currents running into the substrate from the drains or the sources of transistors and affecting other devices. Ideally, the p-bulk is grounded which always reverse biases the p-n junctions at the drains and sources of NMOS transistors *assuming that ground is the lowest voltage that can appear at the drain or source of any transistor*. Similarly, the n-well is connected to V_{DD} to reverse bias the drains and sources of PMOS transistors. However, inductance effects cause overshoots and undershoots which can forward bias these junctions resulting in currents flowing into the substrate causing substrate coupling. For that reason, substrate coupling noise is sometimes called bootstrap noise. Also, if the bulk is biased with a switching ground bus, the ground on the bulk is not perfect because switching transients will cause voltage drops across the line. Hence, the switching transients on the power supply line can couple to transistors resistively through the p^+ bulk contacts. The parallel summation of bulk contacts and epitaxy resistances provides a very low impedance path (nearly short) to the p^+ buried layer.

The second source of substrate noise is capacitive coupling through the MOSFET source and drain p-n junctions. Each n-well on p+ bulk also introduces fairly large p-n junctions forming a capacitance between the V_{DD} rails biasing the n-well and the V_{SS} rails biasing the bulk. The noise injected into the substrate via capacitive coupling is inversely proportional to the rise time of the signals on the drains and sources of transistors. As discussed in the previous section, inductance effects results in faster signal transition times. Another source of substrate noise is impact ionization current, generated at the pinch-off point of the NMOS transistors. Impact ionization causes a hole current in the bulk. A negative bulk transient will increase the depletion region between the source and bulk. This depletes the channel of charge carriers and increase V_{th}. The total effect is a sporadic decrease in the I_{DS} current. In general, these transients increase with higher inductance effects due to the higher voltage swings and overshoots.

C. Requirements on CAD Tools and CAD Tools Performance

The signals that occur in *RLC* circuits are significantly more complicated than signals in *RC* circuits. For example,

the *RLC* signals shown in Fig. 1 have overshoots, very large inertial delay, fast rise time, and are rich in harmonics. Hence, new delay models and model order reduction techniques are required to handle *RLC* circuits. One of the most popular approximate delay models used for the design and analysis of integrated circuits is the Elmore delay model. This first order delay model cannot be used with *RLC* circuits with underdamped responses since under damped responses involve complex poles that appear in conjugate pairs. Hence, at least a second-order approximation is required for *RLC* circuits. One such model was developed in [13] and maintains the popular characteristics of Elmore delay.

Model order reduction techniques allows the calculation of approximations of higher orders to accurately simulate the interconnect. Asymptotic waveform evaluation (AWE) is one popular technique used successfully with *RC* interconnects [24]. However, AWE cannot calculate enough poles to handle complex underdamped responses due to numerical errors. Hence, a set of new model order reduction techniques have been recently developed which are capable of calculating higher order approximations necessary for simulating systems with complex responses. Examples are Pade via Lanczos (PVL) and Matrix Pade via Lanczos (MPVL) [25], Arnoldi Algorithms [26], Block Arnoldi Algorithms [27], Passive Reduced-Order Interconnect Macromodeling Algorithm (PRIMA) [28], and SyPVL Algorithm [29]. However, these model order reduction techniques can have significantly higher computational complexity than AWE. Hence, there is a need for innovative simulation techniques for handling complex responses arising in *RLC* circuits.

Another feature that complicates the analysis and design of integrated circuits including on-chip inductance, is the far reaching inductive coupling to other lines in the integrated circuit. Typically, a line in a wide bus couples to all the lines in the bus. As compared to capacitive coupling, which only couples a line to the immediate neighbors, inductive coupling results in larger circuits (the whole bus rather than three lines) to be analyzed, and these circuits have a significant amount of inputs.

In general, all CAD tools will run significantly slower when using an *RLC* model as compared to an *RC* model. This behavior is simply due to the more complex model used and the higher signal integrity issues involved. In addition to the lower performance of CAD tools, a very large infrastructure of *RC*-based CAD tools needs to be modified to include inductance effects.

V. Conclusion and Future Directions

Currently, the industry applies a three-step design process for integrated circuits when handling inductance. First, employ design methodologies and techniques to reduce the inductance effects in the design. Second, use the well-developed *RC*-based design tools to optimize and verify the circuit. Third, wish nothing will go wrong. However, as discussed in this paper, inductance can have useful effects such as improving the rise time of signals, reducing the power consumption, and reducing the number of inserted repeaters. Hence, by suppressing inductance effects and using *RC*-based tools, a suboptimal circuit results in terms of area, power consumption, and speed. Also, signal integrity and crosstalk issues due to inductive coupling are neglected which can result in undetected reliability problems.

Besides these disadvantages of using *RC*-based tools, this three step solution is only temporary. As discussed in the paper, all the technology scaling trends and technological advances add up to increase inductance effects. Sooner or later, inductance effects will be too hard to suppress or ignore. All the CAD tools for high speed integrated circuit design have to be revised and modified to include inductance. Using an *RLC* interconnect model instead of an *RC* model affects extraction tools, simulation and timing tools, power estimation tools, repeater insertion tools, wire and gate sizing tools, and design methodologies in general.

To be able to include inductance in these CAD tools and in the design process of integrated circuits, it is necessary to develop sound research in several directions. Efficient inductance extraction techniques are of paramount importance to handle large integrated circuits. Model order reduction techniques are necessary that are capable of *efficiently* calculating higher order approximations required to characterize the complicated signals that arise in *RLC* circuits. Design methodologies to optimize *RLC* circuits such as repeater insertion and impedance matching are necessary. Inductive crosstalk estimation and reduction techniques are required to assure reliability. Finally, an intuitive and theoretical understanding of the effects and trends due to inductance has to be developed to help designers make critical design decisions.

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