ASP-DAC 2009 Best Papers

Best Paper Award

1C-1 **FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization**
Gregory Lucas, Scott Cromar, Deming Chen (Univ. of Illinois, Urbana-Champaign, United States)

5C-1 **Efficiently Finding the 'Best' Solution with Multi-Objectives from Multiple Topologies in Topology Library of Analog Circuit**
Yu Liu, Masato Yoshioka, Katsumi Homma, Toshiyuki Shibuya (Fujitsu Laboratories Ltd., Japan)

Best Paper Candidates

1A-1 **Adaptive Inter-router Links for Low-Power, Area-Efficient and Reliable Network-on-Chip (NoC) Architectures**
Avinash Karanth Kodi (Ohio Univ., United States), Ashwini Sarathy, Ahmed Louri, Janet Wang (Univ. of Arizona, United States)

1C-1 **FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization**
Gregory Lucas, Scott Cromar, Deming Chen (Univ. of Illinois, Urbana-Champaign, United States)

3A-1 **System-Level Cost Analysis and Design Exploration for Three-Dimensional Integrated Circuits (3D ICs)**
Xiangyu Dong, Yuan Xie (Pennsylvania State Univ., United States)

4B-3 **Analog Placement with Common Centroid and 1-D Symmetry Constraints**
Linfu Xiao, Evangeline Young (Chinese Univ. of Hong Kong, Hong Kong)

4C-1 **Stochastic Current Prediction Enabled Frequency Actuator for Runtime Resonance Noise Reduction**
Yiyu Shi (Univ. of California, Los Angeles, United States), Jinjun Xiong, Howard Chen (IBM, United States), Lei He (Univ. of California, Los Angeles, United States)

5B-1 **Efficient Analytical Determination of the SEU-induced Pulse Shape**
Rajesh Garg, Sunil P Khatri (Texas A&M Univ., United States)

5C-1 **Efficiently Finding the 'Best' Solution with Multi-Objectives from Multiple Topologies in Topology Library of Analog Circuit**
Yu Liu, Masato Yoshioka, Katsumi Homma, Toshiyuki Shibuya (Fujitsu Laboratories Ltd., Japan)

6B-1 **Efficient Simulated Evolution Based Rerouting and Congestion-Relaxed Layer Assignment on 3-D Global Routing**
Ke-Ren Dai, Wen-Hao Liu, Yih-Lang Li (National Chiao Tung Univ., Taiwan)

7B-1 **Dependent Latch Identification in the Reachable State Space**
Chen-Hsuan Lin, Chun-Yao Wang (National Tsing Hua Univ., Taiwan)

8A-1 **Improving Scalability of Model-Checking for Minimizing Buffer Requirements of Synchronous Dataflow Graphs**
Nan Guan (Northeastern Univ., China), Zonghua Gu (HKUST, China), Wang Yi (Uppsala Univ., Sweden), Ge Yu (Northeastern Univ., China)

8B-1 **A Novel Toffoli Network Synthesis Algorithm for Reversible Logic**
Yexin Zheng, Chao Huang (Virginia Tech, United States)

8C-4 **Design for Burn-In Test: A Technique for Burn-In Thermal Stability under Die-to-Die Parameter Variations**
Mesut Meterelliyoz, Kaushik Roy (Purdue Univ., United States)

Design Contest Award

Best Design Award

1D-1 **A Wireless Real-Time On-Chip Bus Trace System**
Shusuke Kawai, Takayuki Ikari (Keio Univ., Japan), Yutaka Takikawa (Renesas Design Corp, Japan), Hiroki Ishikuro, Tadahiro Kuroda (Keio Univ., Japan)

Special Feature Award

1D-13 **Ultra Low-Power ANSI S1.11 Filter Bank for Digital Hearing Aids**
Yu-Ting Kuo, Tay-Jyi Lin, Yueh-Tai Li (National Chiao Tung Univ., Taiwan), Chou-Kun Lin (ITRI, STC, Taiwan), Chih-Wei Liu (National Chiao Tung Univ., Taiwan)