

# Invited Paper: Overview of 2023 CAD Contest at ICCAD

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## ABSTRACT

The “CAD Contest at ICCAD” is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the field of electronic design automation (EDA). Since 2012, the contest has been publishing many sophisticated circuit design problems, from system-level design to physical design, together with industrial benchmarks and solution evaluators. Contestants can participate in one or more problems provided by EDA/IC industry. The winners will be awarded at an ICCAD special session dedicated to this contest. Every year, the contest attracts more than a hundred teams, fosters productive industry-academia collaborations, and leads to hundreds of publications in top-tier conferences and journals. The 2023 CAD Contest has 210 teams from all over the world, which generates the highest participation record. Moreover, the problems of this year cover state-of-the-art EDA research trends such as circuit verification, hardware security, 3D-IC, and Machine Learning (ML) for EDA from well-known EDA/IC companies. We believe the contest keeps enhancing impact and boosting EDA researches.

## KEYWORDS

CAD Contest, electronic design automation, computer-aided design, circuit verification, hardware security, 3D-IC, ML for EDA

## 1 Introduction

As CMOS technologies continuous to scale down, the specification of modern electronic systems becomes multifarious and stringent, and the IC design complexity has grown dramatically during the past decades. Electronic Design Automation (EDA), or Computer-Aided Design (CAD), is not only a category of software tools for designing electronic systems but also plays an extremely important role to tackle various design challenges, reduce design cycles, and achieve the best trade-off among performance, power, area, reliability, and cost. In order to boost EDA research, the *CAD Contest at ICCAD* [1] offers a platform for industrial companies to share various design problems and design cases while it encourages researchers in academia to study state-of-the-art IC design challenges and advance problem-solving techniques. The contest is a multi-month, research and development international competition, focusing on solving advanced, real-world problems from the industry with both theoretical solutions and practical software.

The CAD Contest was originated as a domestic contest in Taiwan in 1999. It had been a successful annual competition activity, sponsored by Ministry of Education (MOE), Taiwan, for cultivating talented young professionals in the EDA field while contributing to the semiconductor industry. Since 2012, the CAD Contest has been presented at IEEE/ACM International Conference on Computer-Aided Design (ICCAD) [2] – [12], under joint sponsorships of ACM Special Interest Group on Design Automation (SIGDA) [13], IEEE Council on Electronic Design Automation (CEDA) [14], MOE of Taiwan [15], and other industrial companies, including Cadence Design Systems, Inc. [16] and Synopsys, Inc. [17], while the contest environment, including both hardware and software, is supported by Taiwan Semiconductor Research Institute (TSRI) [18]. With the collaborations and between academia, industry, and government, the CAD Contest provide a platform to present modern IC design directions, point out latest challenges, exchange ideas, and build tightly communication links between students, professors, and industry professions.

The contest has already been publishing many sophisticated circuit design problems [19] – [51], from system-level design to physical design, together with advanced design trends such as 3D-IC, Design Space Exploration, AI for EDA, and design for manufacturability in sub-micron technologies. Moreover, the CAD Contest not only contributes to valuable and challenging problems, but also hatch several industrial benchmarks and evaluators for future research. With the precious industrial benchmarks and evaluators, researchers can expend problem scope and conduct valuable study based on these infrastructures.

Contestants from all over the world can participate in one or more problems provided by the industry. The winners will be awarded at an ICCAD special session dedicated to this contest. Every year, the contest attracts more than a hundred teams, fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. It is worth to mentioned that based on the statistics from Google Scholar at September 2023 [52], the CAD Contest special session papers have 591 citations (and 434 citations since 2017), and the h-index is 10. Figure 1 shows the distribution of the citations between 2016 to 2023, and the top five paper with highest citation count.

Note that the number is still growing in 2023. We believe that the contest keeps enhancing its impact and boosting EDA research.

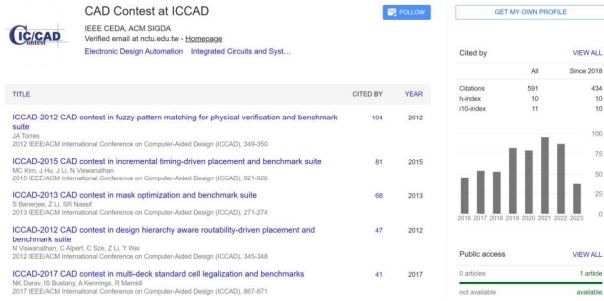


Figure 1. Statistics about CAD Contest at ICCAD related papers from Google Scholar at September 2023 [52].

## 2 Contest Problems

The CAD Contest at ICCAD is a challenging, multi-month, research and development competition. Following the tradition, the 2023 CAD Contest at ICCAD features three critical problems in the fields of front end, back end, and Machine Learning for EDA. The three problems are “**Multi-bit Large-scale Boolean Matching**” provided by Cadence Design Systems, Inc. [49], “**3D Placement with Macros**” contributed by Synopsys, Inc. [50], and “**Static IR Drop Estimation Using Machine Learning**” which is given by a joint collaboration with Arizona State University, Steel Perlot, and The OpenROAD Project [51]. Following we briefly state the major challenges of each problem.

### 2.1 Problem A: Multi-bit Large-scale Boolean Matching

Boolean Matching has been considered as one of the most widely used techniques in the field of logic synthesis, technology mapping, verification, Engineering Change Order (ECO), and even hardware security for hardware Trojan detection. However, with the rapid increasing in the size of modern ICs, the conventional way to negate and permute circuit inputs/outputs become impractical due to high timing complexity. There are several researchers focused on developing efficient Boolean matching algorithms to combat such high complexity. It has been shown that the large number of input/output ports are usually caused by the buses or datapaths in modern designs. If we can know that some inputs/outputs come from the same bus/datapath, we may reduce the complexity of solving the Boolean matching problem by considering the relations between inputs/outputs and the buses/datapaths.

Fig. 2 gives such an example. In the figure, two designs with five input ports and four output ports are given respectively. If we solve the Boolean matching problems by exhaustive search, the number of permutations could be  $5! * 4! = 2880$ . If we know that there are four buses in Circuit I (i.e.,  $\{a0, a1\}$ ,  $\{b0, b1\}$ ,  $\{h0, h1\}$ ,  $\{m0, m1\}$ ) and four buses in Circuit II (i.e.,  $\{x0, x1\}$ ,  $\{y0, y1\}$ ,  $\{u0, u1\}$ ,  $\{w0,$

$w1\}$ ), the problem size can be reduced and the permutations can be significantly reduced to 64.

In this problem, the contestants are asked to find out the matched ports between two given combinational circuits with the information of the list of buses, and the goal is to maximize the number of the matched ports between the two given circuits. We believe this problem can encourage novel ideas about developing efficient algorithms and tools for large-scale Boolean matching problems.

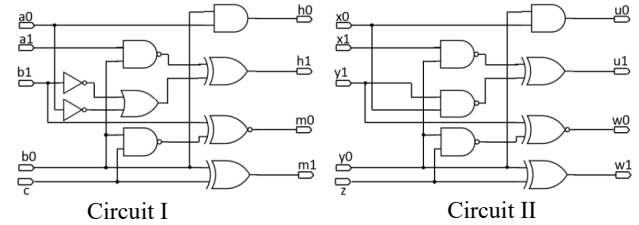


Figure 2. An example to explain that the complexity of Boolean matching problem can be reduced by considering the information of buses [1] [49].

### 2.2 Problem B: 3D Placement with Macros

3D-IC has become promising recently due to the advantages of less power consumption, shorter signal timing, and easier for mixed-signal / mixed-technologies integration. By splitting a large die into two or more small dies and having die-to-die vertical connections, the better yield, better timing, better cost, and even faster time-to-market can be achieved. However, the concept of 3D-IC changes the conventional physical design procedure, where the netlist should be well-partitioned into two dies and interconnections between 2 smaller dies should be carefully designed for maximizing performance and minimized design cost. This leads to a challenging 3D partition and placement problem, and have been modeled and studied in 2022 CAD Contest in ICCAD [47].

On the other hand, modern IC design may apply several semiconductor intellectual properties to speed-up time-to-market, which appears as macros in physical design stage. Usually, the sizes of macros are much larger than standard cells, which lead to significant challenges in circuit placement. We call the design with large macros and smaller standard cells as mixed size design. The challenge become more complicated when applying mixed size design to 3D. In this problem, we focus on 2-die face-to-face vertically stacked configuration with either the same or different technology process on 2 dies.

Contestants are asked to firstly partition the given netlist into 2 dies with the given placement utilization constraints of 2 dies, and then place the macros and legalize std cells for top die and bottom die respectively. The goal is to optimize the given score metrics which include (1) total Half-Perimeter Wirelength (HPWL) of the 2 placed dies, (2) hybrid bonding terminal cost, and (3) runtime cost.

Moreover, several constraints such as non-overlapping, utilization of each die, and the hybrid bonding terminal each inter-die connection can use are need to all satisfied. Figure 3 gives the example of given netlist information and the expected output from the contestants. The problem not only points out a research direction of mixed-size aware 3D-IC design, but also provide several benchmarks as well as an evaluator to provide the correctness checking and quality scoring.

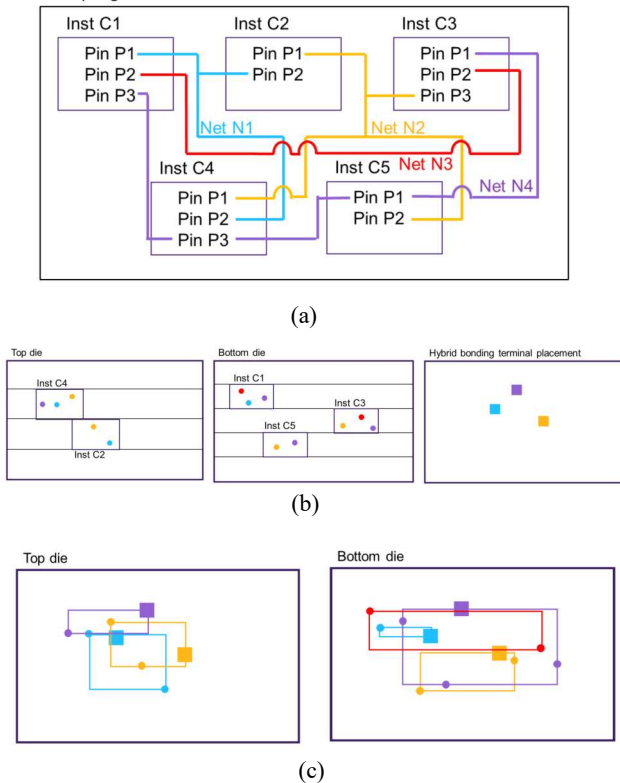


Figure 3. An example of (a) the given netlist, (b) the partition and placement result of top die, bottom die, and hybrid bonding terminal locations, and (c) HPWL result of the output [1] [50].

### 2.3 Problem C: Static IR Drop Estimation Using Machine Learning

IR drop, also known as voltage drop, is always a critical issue to be addressed before the chip can be taped-out. When the voltage supplied to a logic cell decreases, the timing of the cell also changes. The timing change will result in performance loss or violations of setup and hold time for flip-flops, and the timing errors may lead to functional failure and malfunction the chip. Therefore, it is important to check that the worst-case IR drop in the Power Delivery Network (PDN) are within specified limits.

An example of on-chip PDN structure is shown in Figure 4(a). The PDN can be modeled as a network of voltage sources, current sources, and resistances, where the wires are a network of

resistances, the power pad (C4 bumps) are voltages sources connected to the PDN wires, and the current sources are the cells/instances that draw current, as shown in Figure 4(b). Conventionally, static IR drop simulation is performed to estimate where and when the worst-case IR drop may occur by solving a system of linear equations of the form  $GV = J$  where  $G$  is a conductance matrix,  $V$  is the unknown vector of voltages, and  $J$  is the vector of currents. However, considering the high complexity of modern IC designs, it is time consuming or even impractical to solving a bunch of linear equations. Therefore, finding an efficient and effectiveness way to obtain IR-drop information for a given design is in demand.

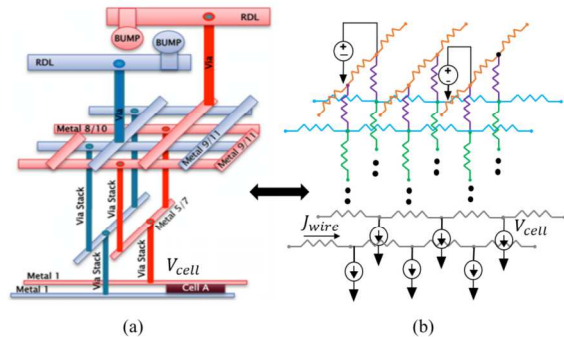


Figure 4. An example of (a) PDN structure and (b) the corresponding model [51].

Recently, researchers proposed to use machine learning models to solve high complexity problems in the EDA field, and some success examples such as DRV predictions and routing congestion estimations are demonstrated to be practical. This contest aims to bypass the computational challenge of static IR drop estimation using machine learning (ML) techniques. Specifically, the goals of this problem are in three fields: (1) Lower the barriers to entry for non-EDA experts by converting a traditional EDA problem to an ML solvable problem and incentivizing the use of novel ML techniques to improve accuracy; (2) Explore the use of transfer learning to address the limited dataset problem in the EDA community; and (3) Establish a state-of-the-art ML model for IR drop prediction.

Specifically, the contestants need to train an ML model to predict static IR drop with the highest possible accuracy (mean absolute error) and F1 score on the test data with the least inference runtime and model size. A large training data set consists of fake dataset from [53] and real-circuit designs are provided, and transfer learning is suggested to the contestants where the initial models are trained using fake data and weights are fine-tuned using real circuit training data, and then the model is tested on validation data (real circuit data only). We believe this problem can inspire various ML-based solutions for IR-drop prediction, which aims to shorten time-to-market and increase circuit performance and yield.

It is worth to mention that the three problems align the research trends in the EDA field nowadays and we believe the three

valuable problems can not only incubate novel ideas and techniques but also attract more talents to join EDA-related research.

### 3 Contest Schedule

The contest starts in February and ends in November. The contestants need to carefully read the problem descriptions as well as reference reading from February, register for the contest by the mid of May, submit their works for alpha, beta, and final stage at June, July, and August, respectively. During the contest period, questions from contestants are well addressed and all Q&As are posted on the official website for contestants' reference. Moreover, testcases or evaluators are provided to all contestants so they can easily verify the correctness and quality. The results from alpha and beta stages are released to each team at following weeks after the submission deadline, and the top X results will be announced on the official website for reference. The final evaluation will take place after the final submission and the winners will be awarded at an ICCAD special session dedicated to this contest. The detailed schedule is shown in Figure 5.



Figure 5. The contest schedules.

### 4 Registration Statistics

The contest this year receives 210 registered teams from 14 countries/regions, including Taiwan, Mainland China, United States of America (USA), India, Hong Kong, Danmark, Russia, Greece, Korea, Brazil, Switzerland, France, Japan, and Germany. Moreover, 3 teams are transnational. Figure 6 shows the numbers of registered teams from 2012 to 2023, and Figure 7 shows the numbers of registered teams of each problem in 2023. From the figures we can observe that the number of participating teams continuous increase since 2021, and this year we reach the highest participation record since 2012. We believe the CAD contests at ICCAD is one of the most impactable contests in the EDA field.

Figure 8 presents the countries/regions where the contestants resides in from 2012 to 2023. From the figure we can find that the 2023 CAD Contest at ICCAD attracts almost double number of countries/regions to participate compared with 2022, which gives the information that the contest problems are on the trend of modern EDA research and can successfully come into focus worldwide.

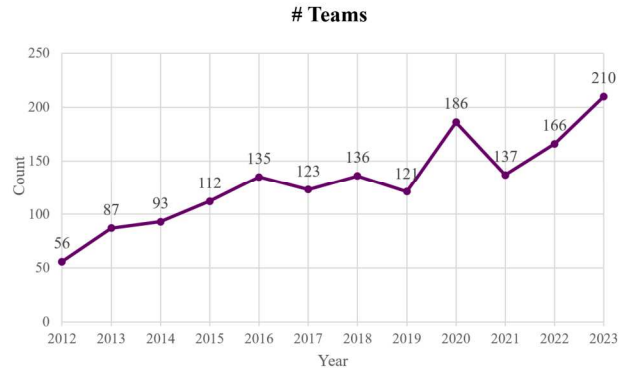


Figure 6. The numbers of registered teams where the contestants reside in from 2012 to 2023.

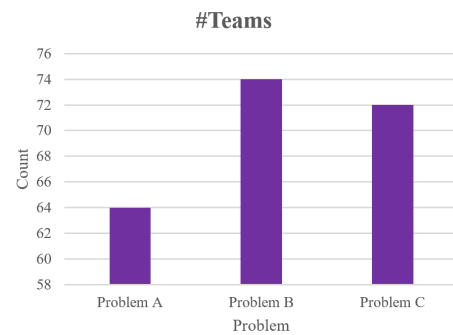


Figure 7. The number of registered teams on each problem at 2023 CAD Contest at ICCAD

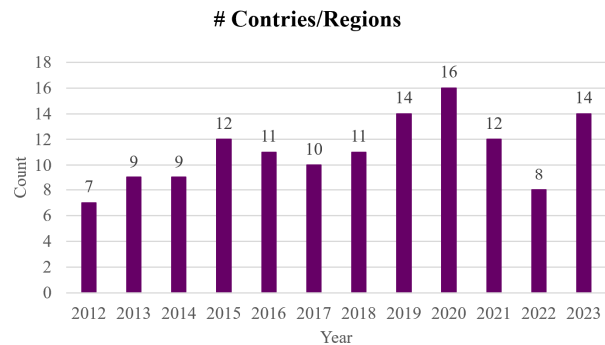


Figure 8. The numbers of countries/regions where the contestants reside in from 2012 to 2023.

### 5 Award Ceremony

The award ceremony is held at 2023 ICCAD special session. The session will give an overview of the 2023 CAD Contest at ICCAD, present the three contest problems of 2023 CAD Contest to the EDA community, announce the contest results, and provide emerging foundations in physical design and ML-CAD research. The session will contain five presentations: The contest chair will first give a brief introduction to the contest. Afterwards, three topic

chairs will introduce each of the contest problems and benchmark suites, announce the contest results, and present awards to the winners. The topic chairs will also play some video clips provided by Top-X teams which present key ideas and algorithms of their solutions to the contest problems. Finally, the Design Automation Technical Committee (DATC) of IEEE CEDA will introduce emerging foundations in physical design and ML-CAD research.

It is worth to mention that the award ceremony in 2020 and 2021 was held as a virtual event due to the serious covid-19 pandemic situation. In 2022, the award ceremony is held as a hybrid event where the winner can participate either in-person or on-line. In this year, the award ceremony is held as an in-person event where the winner can participate on-site for idea future discussions and idea exchanging.

## 6 Conclusions

The CAD contests at ICCAD have presented critical problems and industrial benchmarks to the academic community resulting in research breakthroughs and industry-academia collaborations since 2012. The contest has become one of the largest world-wide academic competitions, and attracted over 1200 international teams during 2012–2023. The published industrial benchmarks have been widely adopted by academia, resulting in numerous publications. The contest keeps enhancing its impact and boosting EDA research.

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