

Synthesis of Reversible Sequential Elements

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To construct a reversible sequential circuit, reversible sequential elements are required. This work presents novel designs of reversible sequential elements such as the D latch, JK latch, and T latch. Based on these reversible latches, we construct the designs of the corresponding flip-flops. Then we further discuss the physical implementations of our designs based on electron waveguide Y-branch switch technology. Test costs, including test generation and test application, of reversible sequential circuits with these reversible flip-flops are also discussed. Compared with previous work, the implementation cost of our new designs, including the number of gates and the number of garbage outputs, is significantly reduced. The number of gates in our designs is 47.4% of the designs in previous work on average. The number of garbage outputs in our designs is 25% of the designs in previous work on average.

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1. INTRODUCTION

Over past 30 years, the trend in microelectronics has been to increase both speed and density by scaling of MOS transistors performing as simple electronic switches. However, this trend will end as we approach the energy barrier due to limits of heat removal capacity on a chip. According to the results reported in Zhirnov et al. [2003], the energy density bound of a two-dimensional system of binary switches is estimated about 5 to 10 million W/cm². By comparison, the power density of the surface of the sun is much lower (roughly

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6000W/cm²). Therefore, it is obvious that the scaling for maximum component densities depends on the heat removal capacity. However, the practical achievable limit of the heat removal capacity for a two-dimensional structure is only about several hundreds W/cm². Therefore, to keep this trend on going, reducing the heat generated during computation process is getting important.

Part of problem of power dissipation (it often causes heat generation) results from the technological nonideality of switches and materials. Therefore, fabrication processes and material technologies have been continually improved to reduce the power dissipation. The other part of the problem arises from Landauer's principle in Bennett [1973] and Landauer [1961], which states that irreversible logic computations necessarily generate at least $kT \log 2$ joules of heat energy for every bit of information loss, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. This part of energy dissipation is independent of the underlying technology. Although power dissipation due to information loss is negligible under current technologies, it will become a substantial part of energy dissipation by 2020 as a result of increased density in computer hardware, if Moore's Law continues to be in effect [Zhirnov et al. 2003].

Reversible computing does not result in information loss during the computation process. Thus, it naturally takes care of heat generated due to information loss. Bennett [1973] shows that zero energy dissipation would be possible only if the gates in a network are all reversible. Reversible computing has been applied to various future technologies as well, such as ultra-low-power CMOS design [Schrom 1998], optical computing [Knill et al. 2001], quantum computing [Nielsen et al. 2000], and nanotechnology [Merkle 1993]. These technologies exploit reversible logic to reduce power consumption.

To realize a function with reversibility, many reversible logic synthesis algorithms have been proposed [Kermtopf 2004; Miller 2002; Miller et al. 2003; Perkowski et al. 2001; Devos et al. 2005; and Yang et al. 2005]. However, most of them address this issue from the aspect of combinational logic. To synthesize reversible sequential circuits, reversible sequential elements such as latches and flip-flops are necessary. Thus, this paper proposes novel designs of reversible sequential elements such as the clocked D latch, clocked JK latch, and clocked T latch. The corresponding flip-flop designs are also introduced.

These reversible sequential elements can be implemented in advanced semiconductor device technology, electron waveguide Y-branch switch technology [Forsberg 2003, 2004, 2005]. In this paper, we will also describe the implementation of these reversible sequential elements using this new nanotechnology.

Testing is an important issue in product development regardless of the underlying technology. We will address the advantages of using our reversible sequential elements for reversible sequential circuit testing.

The remainder of this article is organized as follows. In Section 2, we introduce the background of reversible logic. Section 3 addresses the physical implementation of reversible gates. In Section 4, we review some existing designs of reversible sequential elements. Then we propose new designs of these

x	y	z	x	y	$xy \oplus z$
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

(a)
(b)

Fig. 1. 3-bit Toffoli gate (a) truth table; (b) symbol.

reversible sequential elements and verify their functionalities in Section 5. Section 6 discusses the test cost of the reversible sequential circuit with these new reversible flip-flops. The statistics and comparison of these new designs and previous work are presented in Section 7, and Section 8 concludes the work.

2. BACKGROUND

Definition 1. A gate is reversible if and only if the (Boolean) function is bijective.

A reversible function $f(x_1, x_2, \dots, x_n) \rightarrow (y_1, y_2, \dots, y_m)$ satisfies the conditions of one-to-one and onto mapping between the input and output domains.

Conventional logic gates are almost all irreversible. Among the commonly used gates, only the NOT gate is reversible. The AND and OR gates are irreversible because they violate the requirements of reversible functions. One way to make the AND function reversible is to add one input and two outputs as shown in Figure 1(a). The AND function can be obtained in the third output column $xy \oplus z$ of Figure 1(a), when setting $z = 0$. The truth table of the AND function is shown in bold.

Definition 2. A garbage bit is the additional output that makes an n -input m -output function reversible.

In the reversible AND function shown in Figure 1(a), the outputs x and y are garbage outputs which are used to make the function reversible.

A set of reversible gates is needed to synthesize reversible circuits. Several reversible gates have been proposed in the past. Here we introduce the Toffoli gate and the Fredkin gate, which will be used in our work.

Toffoli gate. The truth table of a 3-bit Toffoli gate is shown in Figure 1(a), and its symbol is shown in Figure 1(b) [Fredkin et al. 1982]. The function of the third column is $xy \oplus z$. That means when $x = y = 1$, the output is z' ; otherwise the output is z . This gate can be used to realize a 2-input reversible AND function by setting z as a constant 0 as mentioned. A Toffoli gate can be generalized as $\text{TOF}(C;T)$, where C is a set of control variables $\{x_1, x_2, \dots, x_{n-1}\}$, T is a target variable $\{x_n\}$ and $C \cap T = \emptyset$. $\text{TOF}(x_1, x_2, \dots, x_{n-1}; x_n)$ is a gate which maps a Boolean pattern $(x_1, x_2, \dots, x_{n-1}, x_n)$ to $(x_1, x_2, \dots, x_{n-1}, x_1x_2 \dots x_{n-1} \oplus x_n)$.

Fredkin Gate. A Fredkin gate is also called a controlled SWAP gate. Figure 2(a) is the symbol of a Fredkin gate, and Figure 2(b) is its truth table [Fredkin et al. 1982]. Its behavior can be described as follows: if the control

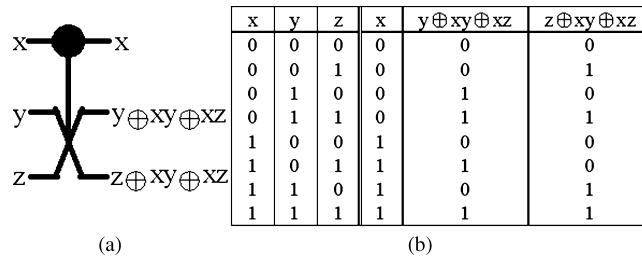


Fig. 2. Fredkin gate (a) symbol; (b) truth table.

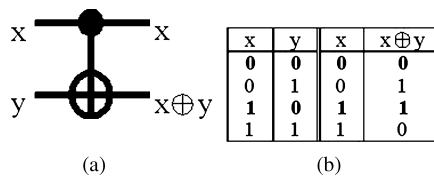


Fig. 3. 2-bit Toffoli gate (a) symbol; (b) truth table.

bit x is set to 1, the outputs of y and z are swapped, otherwise they remain unchanged.

Two restrictions on reversible logic synthesis must be followed [Toffoli 1980]:

- (1) The fanout count of a signal net must equal one. If two copies of one signal are needed, a duplication is necessary.
- (2) A combinational reversible network has to be loop-free. It cannot contain a cyclic path.

The first restriction is in place because a fanout structure is not reversible. For fanout, the input signal number is one, but there are two or more output signals. Therefore, for the first restriction, we use a 2-bit Toffoli gate to duplicate a signal. The symbol of a 2-bit Toffoli gate and its truth table are shown in Figure 3(a) and 3(b), respectively. The function of the second output column is $x \oplus y$. If y is set as a constant 0, a copy of input variable x will be obtained in the second output, which is shown in bold. Therefore, the fanout structure in a conventional network can be implemented in this way.

As for the second restriction, it is required because a reversible combinational function is necessarily a finite one-to-one function. It is customary to express this function in graphical form as a causality network. By construction, causality networks are “loop-free”. Therefore, a combinational reversible network is loop-free.

These two restrictions have to be met in reversible sequential circuits as well. According to Toffoli [1980], a sequential circuit is reversible if its transition function is constructed by reversible logic. Its structure is presented as Figure 4. The transition function in Figure 4 acts as a combinational network. Therefore, the synthesis of this transition function has to conform to the restrictions mentioned.

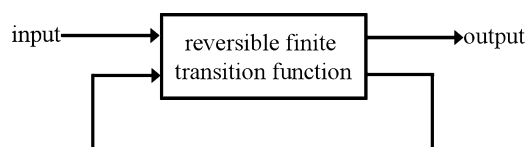


Fig. 4. The structure of a reversible sequential circuit.

There are two objectives in the reversible circuit synthesis.

- (1) Minimize the number of gates. The number of gates gives a simple estimate of the implementation cost of a reversible circuit.
- (2) Minimize the number of garbage outputs. Garbage outputs in reversible circuit add extra implementation costs (area and power). Minimizing the number of garbage outputs leads to minimized area and power.

3. PHYSICAL IMPLEMENTATION OF REVERSIBLE GATES

Some work has proposed the physical implementations of reversible gates, such as Toffoli gate and Fredkin gate, with various technologies [Fredkin et al. 1982; Forsberg 2004, 2003; Melkle et al. 1996]. In this paper, we introduce the electron waveguide Y-branch switch (YBS in the following) technology that can implement our reversible sequential elements. YBS is an advanced semiconductor device technology which has a property of very low power dissipation on switching [Forsberg 2005; Palm et al. 1993]. Thus, it has the potential to use less energy to change state because it turns switch on and off by directing electrons in one of two directions rather than turning the current on or off. Therefore, by using YBS technology, the power dissipation due to nonideality of switches can be reduced. Without charging and discharging behavior, sequential circuit using YBS as the basic cell will be more energy efficient [Forsberg 2005; Palm et al. 1993]. Specifically, YBS approximately dissipates 0.6meV in one switching operation under a normal environment [Forsberg 2005]. This is more than one order of magnitude smaller than the minimum energy cost of one bit information loss at room temperature, $kT \log 2$ is approximately 18meV. Hence, we can expect that the cost of information loss to be a major contributor to the total power dissipation in logic circuits based on YBS.

The schematic of the YBS is shown in Figure 5 [Forsberg 2004]. By creating an electric field perpendicular to a branching waveguide, current from the source is transmitted into the drain with higher electrostatic potential [Forsberg 2004]. Electrons entering the stem from source (1) are deflected to either of the two branches (2 or 3) depending on the direction of the electrical field across the junction applied by the voltage on the controlling gate (G). The electrical symbol of the YBS is shown in Figure 6(a). The direction of the electrical field across the junction thus depends on whether VG is set to VDD or 0. If VG is set to VDD, the value of D1 will be equal to S. If VG is set to 0, D2 will be equal to S. The possible states of the YBS in such a configuration are summarized in Figure 6(b) [Forsberg 2004].

The implementation of reversible gates using YBS technology has been proposed in Forsberg [2003, 2004, 2005]. We take 2-bit Toffoli gate as an example

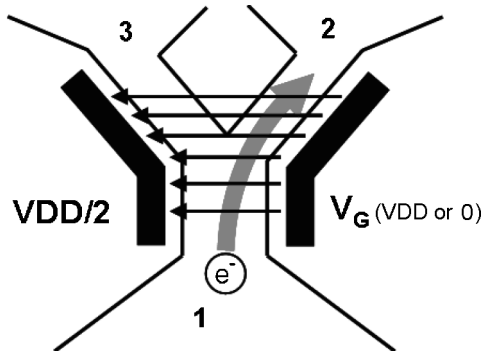


Fig. 5. The schematic of YBS.

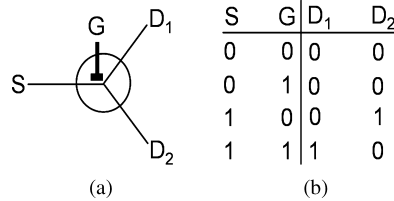


Fig. 6. YBS (a) symbol; (b) state table.

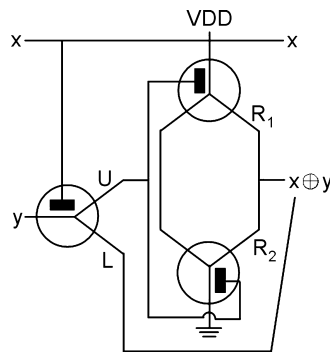


Fig. 7. The implementation of a 2-bit Toffoli gate.

to explain how YBS technology implements reversible gates. The 2-bit Toffoli gate is implemented as shown in Figure 7. According to the functionality of 2-bit Toffoli gate in Figure 3(a), we know the first output of 2-bit Toffoli gate is equal to input variable x . The second output is equal to $x \oplus y$. Therefore, in Figure 7, the first output is simply connected to the input x . As for the second output, when $x = 0$, the value of y will directly pass to the output through lower branch L . When $x = 1$, the value of y will pass to the upper branch U , and if $y = 1$, R_2 branch will be connected to the ground. Therefore, the output node $x \oplus y$ will be 0. On the other hand, if $y = 0$, R_1 branch will be connected to VDD and the output node will be 1. Note that the structure in the right part of Figure 7 acts as an inverter.

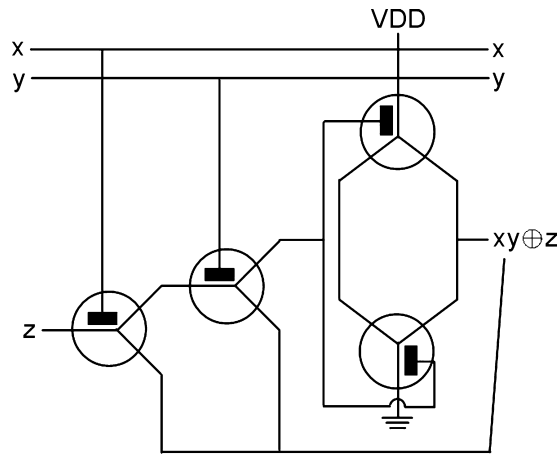


Fig. 8. The implementation of a 3-bit Toffoli gate.

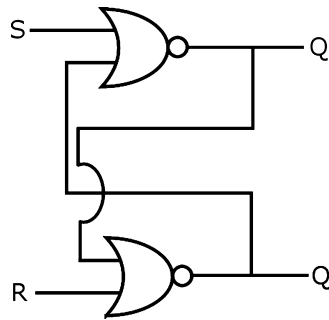


Fig. 9. The traditional RS latch.

According to the functionality of 3-bit Toffoli gate in Figure 1(a), we can also implement a 3-bit Toffoli gate as shown in Figure 8. When $x = 1$ and $y = 1$, the value of z is passed to the inverter and is complemented as the output. When $x = 0$ or $y = 0$, the value of z is directly passed to the output. Since 3-bit Toffoli gate is a universal gate [Perkowski et al. 2001, Toffoli 1980], any reversible function can be constructed using this gate. As a result, any reversible function can be implemented using YBS. Section 5 will give an example to show the implementation of reversible sequential element using YBS.

4. PREVIOUS WORK

Fredkin and Toffoli [1982] discussed topics regarding reversible sequential networks and first introduced a sequential element in the form of the JK flip-flop. However, they did not discuss other popular sequential elements such as the D latch, D flip-flop, etc. Picton et al. [1996] proposed a new design of a reversible RS latch without a clock signal. This work decomposes a clockless RS latch into two conventional NOR gates, as shown in Figure 9. Then each NOR gate is replaced by a Fredkin gate, which can implement the function of a NOR gate. This new RS latch structure is considered reversible because it is constructed

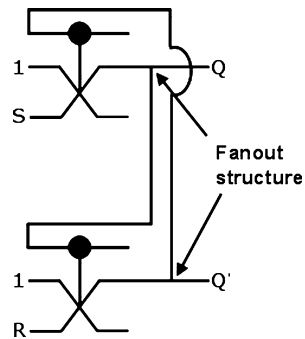


Fig. 10. The reversible RS latch proposed by Picton et al. [1996].

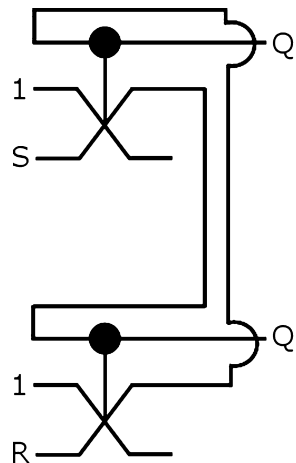


Fig. 11. The reversible RS latch proposed by Rice [2006].

entirely by reversible gates, as shown in Figure 10. However, they also did not discuss other reversible sequential elements.

A recent work proposed by Thapliyal et al. [2005] exploits a similar approach of direct transformation to design other sequential elements such as the D latch, JK latch, etc. In addition, not only the Fredkin gate, but also other reversible gates are used to implement conventional logic gates such as the NOR gate, AND gate, etc. Although many reversible sequential elements are considered in this work, their implementation cost is quite large because these reversible sequential element designs were not further optimized.

Rice [2006] recently proposed a new reversible RS latch design to avoid fanout structures in the original reversible RS latch design proposed in Picton et al. [1996]. The new structure of the reversible RS latch is shown in Figure 11. Moreover, since other sequential elements such as D flip-flop, JK flip-flop, and T flip-flop can be built by an RS latch, this work constructs other reversible sequential elements based on the new design. The direct transformation approach is also adapted in this work to design sequential elements.

Table I. The Truth Table of D Latch

clk	D	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table II. The Augmented Reversible Truth Table of D Latch

clk	D	Q_n	clk'	D'	Q_{n+1}
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

These three works all use the direct transformation approach to design reversible sequential elements. Direct transformation approaches, however, require a large number of gates and garbage outputs. Therefore, this paper proposes a new approach for the construction of reversible sequential elements.

5. NOVEL DESIGNS OF REVERSIBLE SEQUENTIAL ELEMENTS

This section presents our new designs of reversible sequential elements. Also, our approach for getting these results is introduced in detail.

5.1 Clocked Reversible Latches

Our synthesis method is a truth table extension method. Unlike the direct transformation-based method, we do not replace irreversible gates with the reversible ones within a sequential element. Instead, we extend the original irreversible truth table of a sequential element to an augmented reversible one. We take the D latch as an example. First, we get the truth table of the D latch and make it reversible. The truth table of the D latch in Table I is not a reversible function, since the mapping between the input and output domains is not one-to-one. Therefore we have to add garbage outputs to make it reversible. The minimum number of garbage outputs required for reversibility is $\lceil \log(q) \rceil$, where q is the maximum number of times an output pattern repeated in the truth table Maslov et al. [2003]. In this case, 0 and 1 are repeated 4 times in the output column $Q_n + 1$. Therefore, we add $\lceil \log(4) \rceil = 2$ output variables clk' and D' in the truth table and make the table reversible as shown in Table II. Note that different values assigned to these two output columns will affect the result of our design. Under our assignments in Table II, we observe that

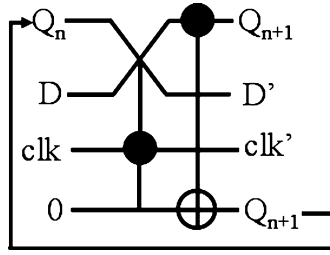


Fig. 12. The complete implementation of reversible D latch.

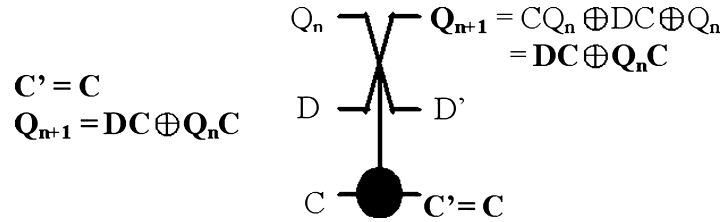


Fig. 13. Functional verification on reversible D latch.

Table II is identical to Figure 2. Thus, a D latch can be modeled by a Fredkin gate. This means we only need one Fredkin gate to implement a reversible D latch. However, if we assign these values in different ways, the design may be different.

Compared with previous work, if we use a direct transformation method to implement a reversible D latch, the synthesis result would not be good because a traditional D latch is built by many irreversible gates, and using the direct transformation method to construct a reversible D latch requires a large number of gates and garbage outputs.

After synthesizing this augmented reversible function, we consider the fanout problem. The input Q_n in the next state comes from the current output Q_{n+1} . Thus, an additional Q_{n+1} is needed for feedback. Here a 2-bit Toffoli gate is used to duplicate the output variable Q_{n+1} . The final structure of the D latch is shown as Figure 12.

We verify that this reversible D latch design exactly implements the behavior of a D latch. The leftmost part of Figure 13 shows the Boolean functions obtained from the augmented truth table of the D latch in Table II. To simplify the expression of Boolean equations, the symbol “C” is used to represent input variable clk . The rightmost part of Figure 13 shows the functions of the implemented reversible D latch. These two expressions are identical, therefore, the functionality of our reversible D latch is correct.

Similarly, a reversible T latch can be modeled as a Toffoli gate using the same method. The implementation of a reversible T latch is shown in Figure 14(a). Figure 14(b) shows the verification result, and Figure 14(c) shows the augmented truth table.

As for the JK latch, it is difficult to model its function using a single reversible gate because its function is quite complex. Therefore, we exploit a transformation-based synthesis algorithm [Miller et al. 2003] to construct the

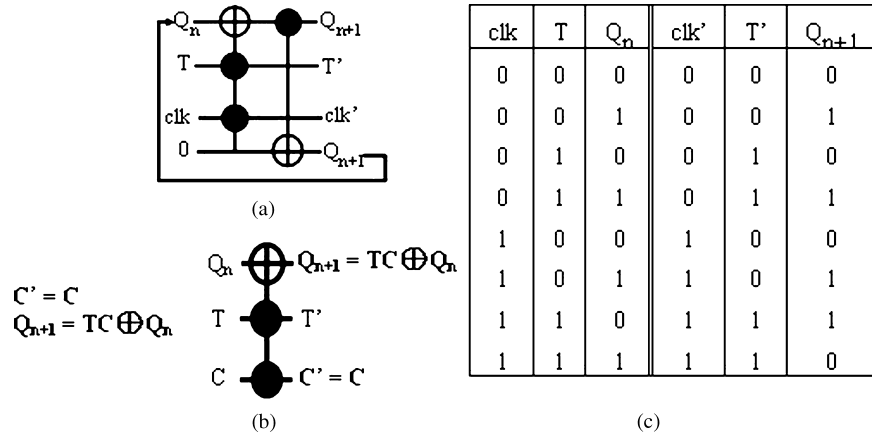


Fig. 14. T latch (a) structure; (b) functional verification; (c) the augmented truth table.

Table III. The Augmented Reversible Truth Table of JK Latch

clk	J	K	Q_n	clk'	J'	K'	Q_{n+1}
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

reversible JK latch. First, we also derive the augmented reversible truth table as shown in Table III. Then, we apply the transformation-based synthesis algorithm to implement the reversible function. The philosophy of the transformation-based algorithm is to cascade some reversible gates such that the output of the truth table is equal to the input. Next, we describe how to construct our reversible JK latch in detail.

First, we inspect the augmented truth table in lexicographical order until an output assignment differs from the input assignment. In Table III, the first output assignment that is not equal to the input assignment is 1110.

Then we add some generalized Toffoli gates from the end of the constructed circuit towards its beginning to make the output assignments equal to input assignments. There are two rules for choosing a generalized Toffoli gate.

In	Out	S1	S2	S3
0000	0000	0000	0000	0000
0001	0001	0001	0001	0001
0010	0010	0010	0010	0010
0011	0011	0011	0011	0011
0100	0100	0100	0100	0100
0101	0101	0101	0101	0101
0110	0110	0110	0110	0110
0111	0111	0111	0111	0111
1000	1000	1000	1000	1000
1001	1001	1001	1001	1001
1010	1010	1010	1010	1010
1011	1110	1111	1011	1011
1100	1101	1100	1100	1100
1101	1011	1011	1111	1101
1110	1111	1110	1110	1110
1111	1100	1101	1101	1111

Fig. 15. The synthesis process of reversible JK latch.

- (1) Deal with the bits that should become 1 first. We want to change the output assignment 1110 to 1011. Hence the 2nd bit should be changed from 1 to 0 and the 4th bit should be changed from 0 to 1. Therefore, we deal with the 4th bit first.
- (2) Keep the output assignments prior to the current one intact. The output assignments prior to 1110 are identical to their corresponding input assignments, so we leave them unchanged. Either $\text{TOF}(\text{clk}', J', K'; Q_n + 1)$ or $\text{TOF}(\text{clk}', J'; Q_n + 1)$ is effective for inverting the 4th bit of 1110 and leaving the output assignments prior to it unchanged. In our design, we choose a $\text{TOF}(\text{clk}', J'; Q_n + 1)$ and add it to the end of the constructed circuit in this iteration. Note that this process might change other output assignments after 1110, such as 1101 or 1111. Nevertheless, we can reform them in the same way in later iterations.

In each step, we choose an appropriate generalized Toffoli gate to synthesize the reversible function according to these two rules. The algorithm is terminated when all of the output assignments are equal to the input assignments. Figure 15 shows the process of synthesizing this reversible JK latch. After adding a generalized Toffoli gate in each step, changed output assignments are shown in bold. Note that the gates are identified sequentially from the output side to the input side. The resulting circuit has to be reversed and is shown in Figure 16(a), and the final structure of the reversible JK latch is shown in Figure 16(b). The verification of the reversible JK latch is shown in Figure 17. We use Figure 18 to illustrate the structure of a reversible sequential circuit with the new proposed reversible D latches. The combinational part and the sequential elements of a reversible sequential circuit also have to be reversible. The clock signal of each reversible sequential element will be pulsed by a global clock source.

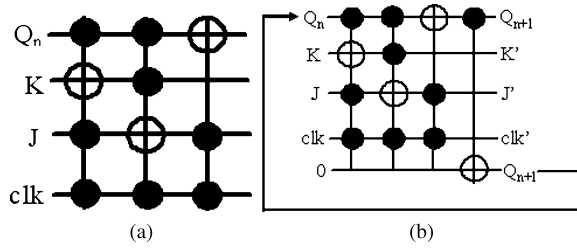


Fig. 16. JK latch (a) the reversible transition function; (b) the complete implementation.

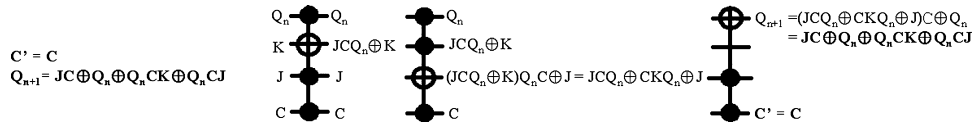


Fig. 17. Functional verification on reversible JK latch.

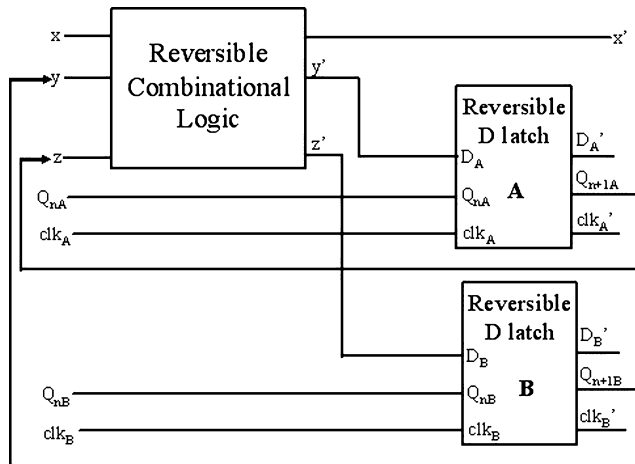


Fig. 18. An illustration of reversible sequential network.

5.2 Clocked Reversible Flip-Flops

A flip-flop is an edge-triggered sequential element while a latch is a level-sensitive sequential element. A traditional D flip-flop consists of two D latches and one inverter, as shown in Figure 19, [Mano 1988]. The first D latch is called the master and the second one is called the slave. Since a reversible D latch has been built, a reversible D flip-flop can be constructed directly by replacing the D latches and inverter with its reversible versions. Here we do not use truth table extension method to construct flip-flops. This is because we cannot extend the truth table that contains edge-triggered behaviors. Therefore, we imitate the traditional method of designing flip-flops, combining two latches with gates, to realize the reversible flip-flops. The behavior and structure of a reversible D flip-flop are shown in Figure 20(a) and (b), respectively. We can trace the D flip-flop design and compare the function with its truth table. The behavior of

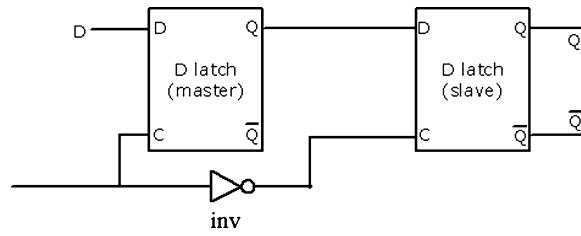
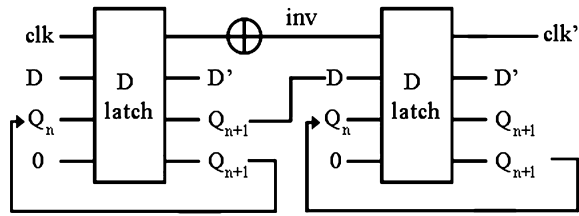


Fig. 19. An irreversible conventional D flip-flop.

clk	D	Q_{n+1}
0	*	Q_n
1	*	Q_n
\downarrow	0	0
\downarrow	1	1

(a)

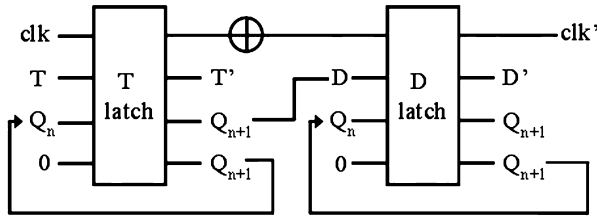


(b)

Fig. 20. D flip-flop (a) behavior; (b) structure.

clk	T	Q_{n+1}
0	*	Q_n
1	*	Q_n
\downarrow	0	Q_n
\downarrow	1	$\overline{Q_n}$

(a)



(b)

Fig. 21. T flip-flop (a) behavior; (b) structure.

the implemented D flip-flop is the same as that of the truth table in Figure 20(a). The implementations of reversible T flip-flop and JK flip-flop are shown in Figures 21 and 22, respectively.

Based on these existing implementations of reversible gates, we can construct our reversible sequential elements. We take our reversible T latch design in Figure 14(a) as an example. Our reversible T latch design consists of one 3-bit Toffoli gate and one 2-bit Toffoli gate. Since the 3-bit Toffoli gate and 2-bit Toffoli gate have been built, a reversible T latch can be directly constructed as

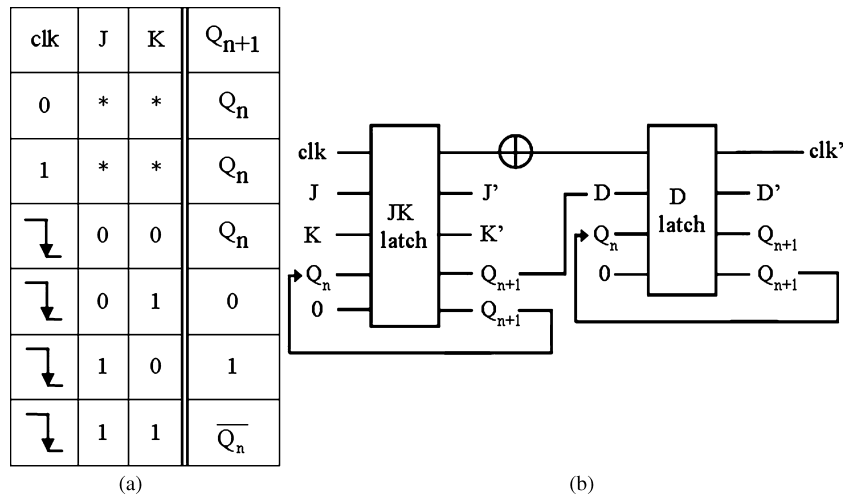


Fig. 22. JK flip-flop (a) behavior; (b) structure.

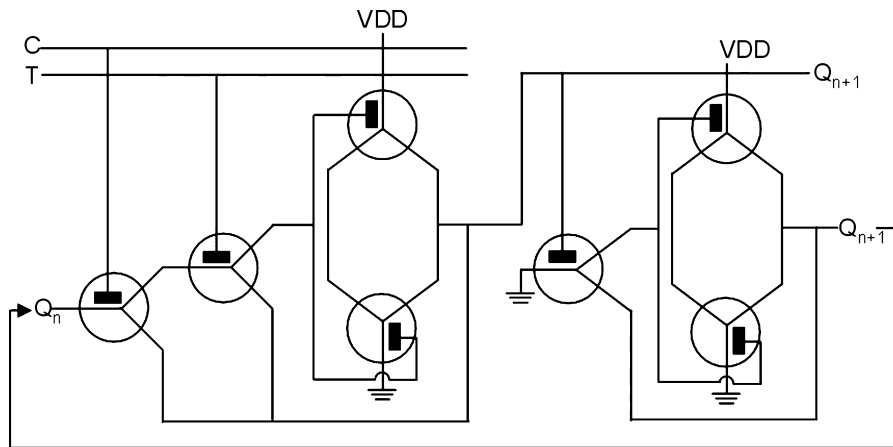


Fig. 23. The implementation of a reversible T latch.

shown in Figure 23. In Figure 23, the left part is a 3-bit Toffoli gate and the right part is a 2-bit Toffoli gate.

6. DISCUSSION OF TEST COST IN REVERSIBLE SEQUENTIAL CIRCUITS

Testing on combinational reversible circuits have been proposed in Patel et al. [2003] and Hayes et al. [2004]. However, no previous work considers the testing issue in reversible sequential circuits. Therefore, in this section, we will discuss the test cost in reversible sequential designs.

The test cost of a circuit consists of the costs of test generation and test application. In traditional sequential circuits, we insert scan chains into designs to improve the controllability and observability of internal states [Williams et al. 1982, 1973]. Thus, the cost of test generation is reduced. However, the

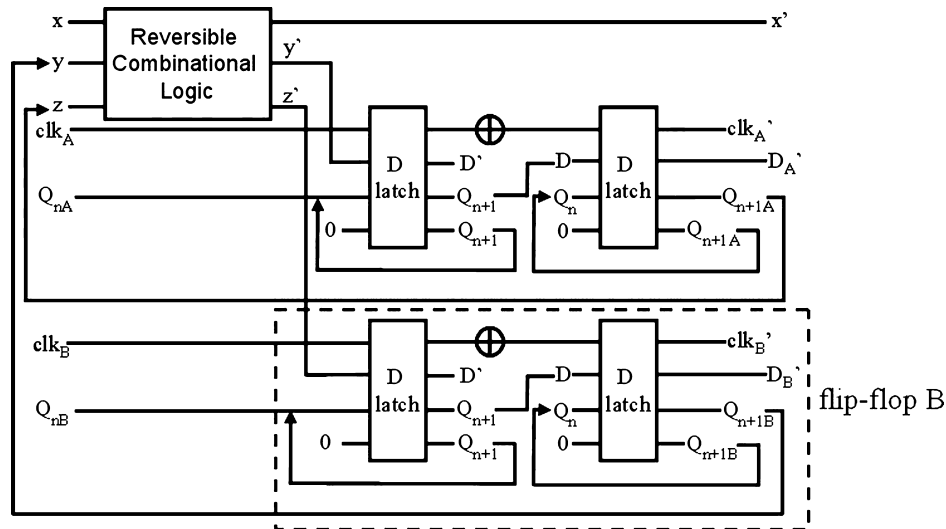


Fig. 24. The reversible circuit with the proposed D flip-flops.

cost of test application is still large due to a long sequence of scan operations that shift values in and out of scan chains.

Reversible function satisfies the conditions of one-to-one and onto mapping between the input and output domains. This property fundamentally affects testing of reversible circuits, making it significantly simpler than for the irreversible case [Patel et al. 2003]. For example, “there exists a test vector that generates any desired state on any of the circuit” is an important testing property that only holds in reversible circuits [Shahin 2005]. This property significantly reduces the test generation cost Patel et al. [2003]. There are some other properties on reversible circuit testing which are summarized in Patel et al. [2003] and Shahin [2005].

The property mentioned above, “there exists a test vector that generates any desired state on any of the circuit,” also holds for the proposed reversible sequential elements. Therefore, we can easily set any desired output state from the input of the reversible sequential elements.

Although we mentioned that reversible circuits have the property of easily setting any desired output state, this property is not directly useful to reversible sequential circuits. This is because for sequential circuits, the outputs are not completely controlled by the primary inputs. They are also affected by the states of flip-flops. If the states of sequential elements are not easy to be set, the cost of test generation would not be reduced. Of course one can still insert scan chains to achieve the state setting in reversible sequential circuits.

The proposed reversible D flip-flop has an input Q_n . We can improve the controllability of internal states through Q_n without inserting scan chains. Figure 24 shows a reversible sequential circuit with proposed reversible D flip-flops. In Figure 24, there are two reversible D flip-flops A and B. Each one has its own clk , Q_n , and Q_{n+1} signals. Under our reversible sequential designs, we can apply signal at the primary input Q_n to directly set internal states.

Table IV. The Statistics and Comparison of Our New Designs and Previous Work [Thapliyal et al. 2005]

Types	NO. of Gates			NO. of Garbage Outputs		
	Ours	Thapliyal et al. [2005]	Ratio (%)	Ours	Thapliyal et al. [2005]	Ratio (%)
D latch	2	7	28.6	2	8	25.0
JK latch	4	10	40.0	3	12	25.0
T latch	2	10	20.0	2	12	16.6
D flip-flop	5	—	—	3	—	—
JK flip-flop	7	18	38.9	4	21	19.0
T flip-flop	5	—	—	3	—	—
Average	—	—	31.9	—	—	21.4

For example, in Figure 24, we assign the internal state at the primary input Q_nA and Q_nB . According to Figure 24, the primary outputs of the reversible D flip-flops $Q_{n+1}A = Q_nA$ and $Q_{n+1}B = Q_nB$, which means that we have set an internal state into the reversible D flip-flops and the reversible sequential circuit will work immediately under this specific state. Thus, the cost of test application in reversible sequential circuits using our designs is lower than that of traditional scan design approaches. No matter how many reversible D flip-flops are connected with the reversible combinational logic in Figure 24, we can directly set one test vector into all reversible D flip-flops for current state values without using a long sequence of operations to shift values into these reversible flip-flops.

Next we further discuss the test costs using direct transformation-based reversible D flip-flops [Rice 2006]. The structure of the direct transformation-based reversible D flip-flop is quite similar to the conventional D flip-flop, its primary inputs are only D and clk. Thus, the only way to set internal states into this reversible D flip-flop is through the input D. However, we know that the value of input D is the output of the reversible combinational logic. Therefore, it is not trivial to get any desired internal state using the direct transformation-based reversible D flip-flops. Consequently, using direct transformation-based reversible D flip-flops is not beneficial to reduce the test cost of the reversible sequential circuits.

7. THE DISCUSSION OF RESULTS

Tables IV and V show the statistics and comparison of our new designs against those proposed in Thapliyal et al. [2005] and Rice [2006], respectively. In these two tables, column 1 shows the types of the sequential elements. We use the number of gates and the number of garbage outputs as the cost functions to measure the quality of a design. Each table is separated into two parts by these two costs and each part has three columns. In Table IV, the column “Ours” shows the cost of our design. The column “Thapliyal et al. [2005]” shows the cost reported in Thapliyal et al. [2005]. The column “Ratio” is the percentage of Ours/Thapliyal et al. [2005]. For example, for a D latch design, our implementation has 2 gates while Thapliyal et al. [2005] has 7 gates. Thus, the ratio is $2/7 = 28.6\%$. The last row “Average” shows the average ratio among these different reversible sequential elements.

Table V. The Statistics and Comparison of Our New Designs and Previous Work [Rice 2006]

Types	NO. of Gates			NO. of Garbage Outputs		
	Ours	Rice [2006]	Ratio (%)	Ours	Rice [2006]	Ratio (%)
D flip-flop	5	11	45.5	3	12	25.0
JK flip-flop	7	12	58.3	4	14	28.6
T flip-flop	5	13	38.5	3	14	21.4
Average	—	—	47.4	—	—	25.0

Rice [2006] did not summarize the number of gates and the number of garbage outputs of their reversible sequential elements. We count these numbers based on their designs and show them in Table V.

According to the statistics in Table IV and Table V, the implementation cost of our designs is lower than those of Thapliyal et al. [2005] and Rice [2006]. For example, with the number of gates in reversible JK flip-flop, our cost is only 7, compared to 18 with Thapliyal et al. [2005] and 12 with Rice [2006]. With the number of garbage outputs in reversible JK flip-flop, our cost is only 4, compared to 21 with Thapliyal et al. [2005] and 14 with Rice [2006].

8. CONCLUSIONS

This paper proposes novel designs of basic reversible sequential elements such as latches and flip-flops. The design process is also introduced in detail. As comparing with previous work, the implementation costs of these new designs are more competitive. Thus, the resulting reversible sequential circuits are more cost efficient. To consider the power dissipation due to nonideality of switching, we also introduce an advanced switching device, electron waveguide Y-branch switch, as the basic cell of our new designs. With this implementation, the power consumption of these reversible designs can be controlled and kept arbitrarily low. Furthermore, the testing issue in the reversible sequential circuits using our designs is discussed.

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